

C2900 Repair Guide

Prepared by	Chen Taojie/54908	Date	2007-1-18
Reviewed by		Date	
Approved by		Date	
Authorized by		Date	



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Contents

1 C2900 Description	1-1
1.1 Introduction to the Phone.....	1-1
1.2 Specifications and Indexes of the Hardware and Software	1-2
2 Phone Principium	2-1
2.1 Functional Modules and Service Descriptions of the C2900	2-1
2.2 Description of Functional Circuits	2-2
2.2.1 Power-On and Power-Off Working Principles	2-2
2.2.2 Baseband Unit	2-3
2.2.3 Radio Frequency Unit.....	2-6
2.2.4 Power Supply/Reset/Charge Management.....	2-7
2.2.5 Peripheral Circuit	2-11
3 Functional Chip.....	3-22
3.1 Core Chipset	3-22
3.2 FM Chip.....	3-23
4 Assembling Description	4-1
4.1 C2900 Explosion Diagram.....	4-1
4.2 Assembling	4-2
5 Troubleshooting.....	5-1
5.1 No Vibration.....	5-1
5.2 No Display of LCD	5-2
5.3 "Check UIM" is displayed after the phone is powered on.....	5-3
5.4 No Ringtone.....	5-4
5.5 No sound is heard after the call is set up.....	5-5
5.6 The other party cannot hear you after the call is set up.....	5-6
5.7 No sound is heard while using the earpiece.	5-7
5.8 No sound is sent while using the earpiece.....	5-8
5.9 Press the button on the earpiece to answer a call is ineffective.	5-9
5.10 No Charging.....	5-9
5.11 The phone cannot be powered on.	5-11
5.12 Key Failure	5-16
5.13 No Signal	5-17

5.14 Weak Signal5-21

5.15 FM Failure5-22

6 Appendix..... 6-1

6.1 Unused Pad of the BGA..... 6-1

6.2 Networks to the Test Point 6-1

6.3 Acronyms and Abbreviations 6-2

1 C2900 Description

1.1 Introduction to the Phone

The C2900 mobile phone (hereinafter referred to as the C2900) adopts the Qualcomm QSC6010 platform, which provides CDMA2000 1X terminals with a highly integrated solution. By using the QSC6010 chips, the phone supports the CDMA800M mode, but does not support GPS. It also supports the FM radio.

The C2900 is equipped with the 128 × 128 pixel CSTN LCD. It provides IO connectors (including the charger interface, serial port, JTAG interface and earphone interface) and the R-UIM interface, as well supports 32 poly-phonic ringtones and the vibration mode. Powered by a Li-Ion battery of 850 mAh, the phone supports the standby time for 230–270 hours and continuous talk-time for 4.5–5.0 hours. The antenna of the phone is build-in.

Figure 1-1 shows the appearance of the C2900.

Figure 1-1 C2900 appearance



1.2 Specifications and Indexes of the Hardware and Software

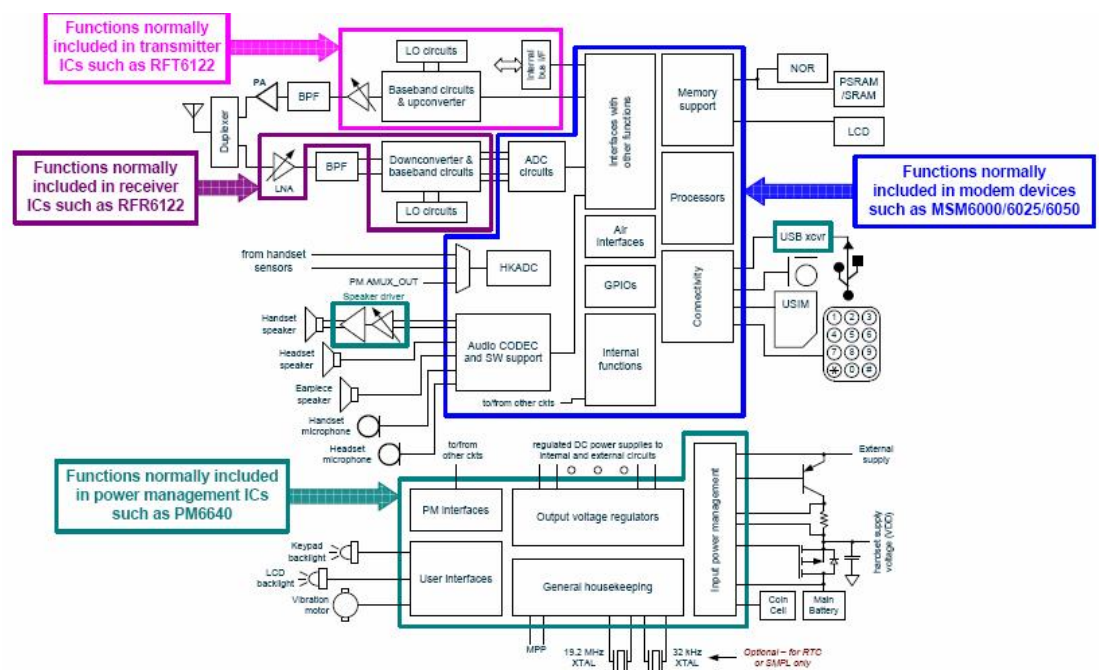
Item	Specification
Shape	Bar-type
Dimensions (L × W × H)	103 mm × 43.4 mm × 14 mm
Weight	About 75 g (including the battery)
Antenna	Built-in
UIM	Supporting the R-UIM and the ROM-UIM modes

Item	Specification	
Interface	Charger interface: 24 pin	
	Earphone interface: 24 pin	
Battery	850 mAh Li-ion	Standby time: 230–270 h (depending on the network)
		Talk time: 270–310 min (depending on the network)
Display	Type	CSTN
	Size	1.5 inch
	Color	Color display
	Pixel	128 × 128
Keypad backlighting	Blue	
Technical specifications	CDMA 1xRTT Release 0 3GPP2 Release0 (1999.7) plus Addendum 2 (August 2001) IS-95 A/B compatible IS98D IS-683A	
Frequency band	† Transmission: 824–849 MHz † Reception: 869–894 MHz	
Temperature	† Working environment: –10°C to +55°C † Storage environment: –20°C to +70°C † Transportation environment: –20°C to +70°C	
RF performance specifications	† Maximum transmission power: ≥ 23.5 dBm/1.23 MHz † Reception sensitivity: –104 dBm/1.23 MHz or less (FER=0.5% with 95% confidence)	
Language	† First software version: Chinese and English (Unicom version) † Second software version: Hindi and English (TATA version) † Future versions: Spanish, Arabic, and Portuguese (decided by considering the market trend)	
Storage capacity	61 Mbit (Flash) + 16 Mbit (RAM)	

2 Phone Principium

2.1 Functional Modules and Service Descriptions of the C2900

Figure 2-1 Diagram of the C2900 Functional modules



As shown in Figure 2-1, there are mainly three functional modules of the C2900.

- I Baseband module: It includes the baseband unit of the QSC6010, memory, LCD, FM(TEA5767HN), various external connectors (IO, UIM card slot, JTAG, earpiece interface), audio processing module (MIC, receiver, speaker, audio amplifier, earpiece amplifier), and keypad.
- I Power management: It includes the power management of QSC6010, which controls the power of all the phone modules (input power and output voltage), housekeeping management, users, and IC interfaces. The mentioned housekeeping management

provides the following functions: gaining and compensating the adjustable analog multiplexers, system clock circuits, and over-temperature protection.

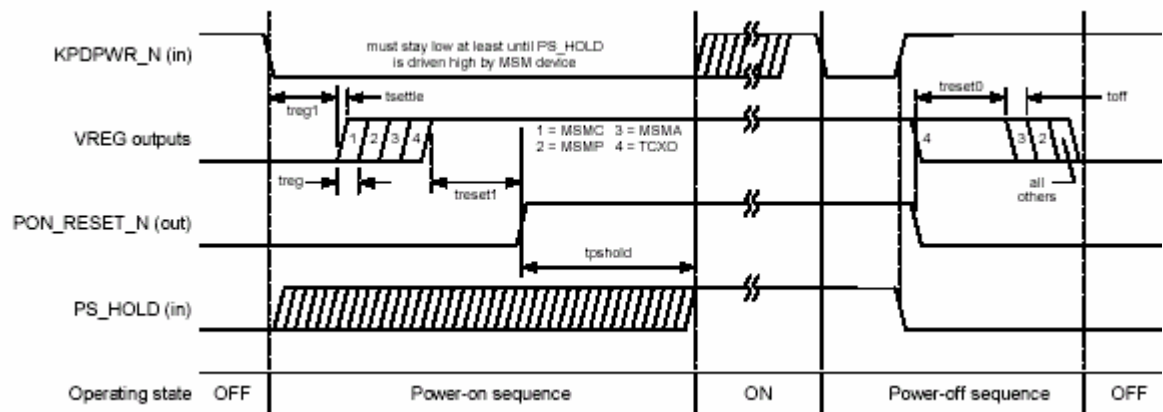
- I RF module: The RF unit of the QSC6010 includes the RF front end, RF-to-baseband receiver, baseband-to-RF transmitter, power amplifier module. The functions of the RF module are as follows: amplify the received RF signals and demodulate them into baseband I/Q signals. Then they can be processed by the baseband; or modulate the baseband analog signals–I/Q signals into RF signals. Then they are transmitted after being filtered and amplified.

2.2 Description of Functional Circuits

2.2.1 Power-On and Power-Off Working Principles

- I Power-On Sequence

Figure 2-2 Power-on sequence



If any of the events is triggered, PM executes the following power-on sequence:

1. Any of the two events occurs, or both events occur continuously.
2. Briefly validates the power supply – an external power supply or main battery is connected.
3. Checks that the internal voltage reference is valid.
4. The power supply is connected to VDD.
5. Checks the rising VDD voltage. If the UVLO threshold is reached, the power-on process continuous.
6. Checks that the voltage controllers (MSMP, MSMC, MSMA, and TCXO) whose default status is on are valid, PON_RESETB output is decreased and MSM is reset.
7. Checks the voltage of VREG_MSMP and VREG_MSMC to make sure that voltage rises to the valid range.
8. Starts the PON_RESET counter. If PON_RESET counter stops, PON_RESET output rises.
9. Starts the PS_HOLD counter and continuously monitors MSM PS_HOLD signals. If PS_HOLD signals increases before PS_HOLD stops, the power-on sequence completes.

- If PS_HOLD signals rise before PS_HOLD counter stops, the status of PM switches to on. An interruption is generated and sent to MSM to judge which is the trigger event.
- If the PS_HOLD counter stops, the status of PM switches to off. The power-on sequence is back to step 1. If there is still one trigger event, the power-on sequence continues.

After a power-on completes, the status of PM is always on, unless MSM decreases PS_HOLD signals or UVLO occurs (VDD value is lower than the threshold). When any of the two events occurs, the power-off sequence will be executed.

I Power-Off Sequence

When MSM is powered on and working, if the Power key is pressed, a power-off sequence is initiated.

The KPD_PWR_N connects to the Power key of the phone and increases internally. The Power key is multifunctional. For example, the Power key can be used to end a call or power on/off the phone.

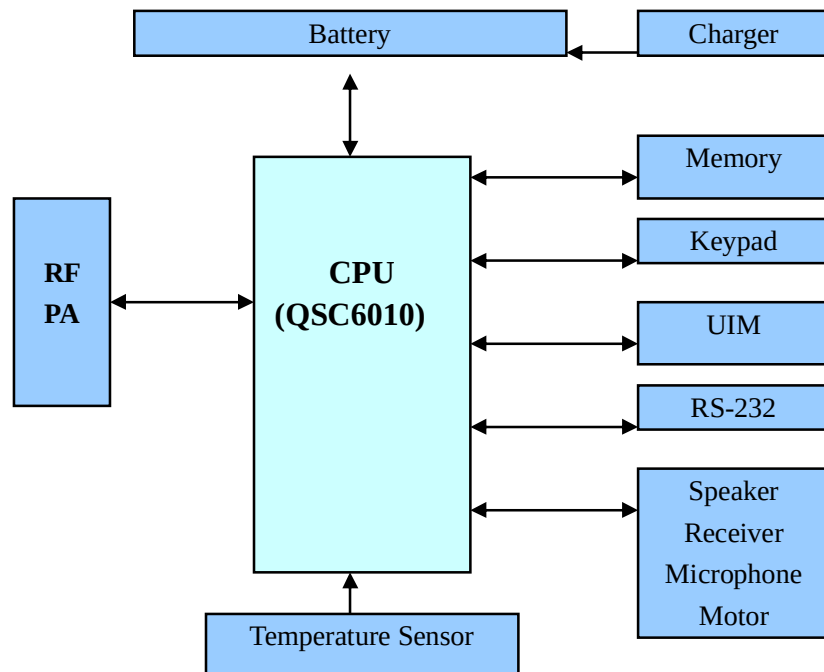
MSM checks the Power key through internal logic. If KBDPWR_N is interrupted, it initiates a power-off sequence:

1. Make sure that the **END** key is pressed and held for at least two seconds. Otherwise, the power-off sequence aborts.
The phone displays a prompt, such as “Power off...”.
2. The phone writes information into the Flash ROM.
3. Wait until the user releases the **END** key. Otherwise, the PM is in the power-on status again.
4. Driver PS_HOLD signals are low. Then PM powers off the phone.

PM responds to UVLO and immediately initiates a power-off sequence. The function protects the battery.

2.2.2 Baseband Unit

Figure 2-3 shows the functional diagram of the baseband unit. The core chipset QSC6010 processes baseband signals and also functions as user interfaces.

Figure 2-3 Functional diagram of the baseband unit

Core chipset

Implemented with the ZIF technology, the QSC6010 chipset provides CDMA2000 1X terminals with highly integrated solution.

The QSC6010 baseband processing sub-system includes the audio CODEC unit, baseband signal processing unit, and CPU of running protocol software. All the functional units are integrated in the QSC6010.

The memory adopts the MCP storage chip of Samsung (Model:K5A6317CTM-D770000, with 32 Mbit Multi-bank Flash and 16 Mbit SRAM). The memory provides the operating system of QSC6010 with the codes, file system and data storage space. (The model of the memory may be different.)

The MCP connects with the QSC6010 through data bus, address bus, and control cable. The Flash and SRAM share the address bus A0–A20 and the 16-bit data bus. The FLASH chip select is EBI_CS_N0, and the SRAM chip select is EBI_CS_N6. The following is the information for other control cables:

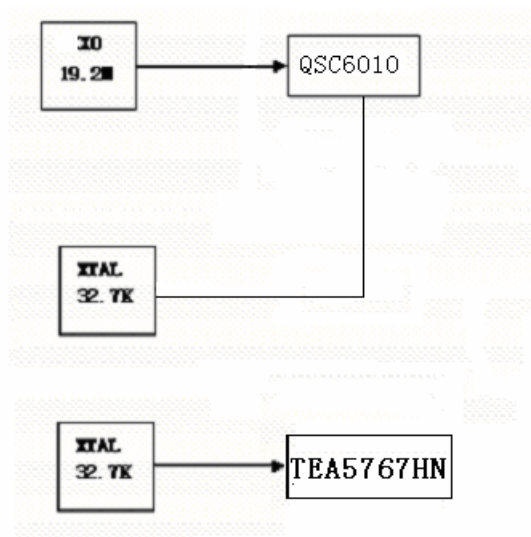
- ┌ EBI_LB_N—>/LBs: The lower eight bits of SRAM data bus are valid.
- ┌ EBI_UB_N—>/UBs: The upper eight bits of SRAM data bus are valid.
- ┌ EBI_OE_N—>/OE: Read enabling signals.
- ┌ EBI_WE_N—>/WE: Write enabling signals.
- ┌ EBI_RESOUT_N—>/RESET: Reset signals.

The voltage of IO interfaces between the QSC6010 and the MCP is set to VREG_MSME2 (2.9 V). The QSC6010 has 25 address lines (A0–A24). With the 64Mbyt addressing capability, its scalability is powerful.

Clock

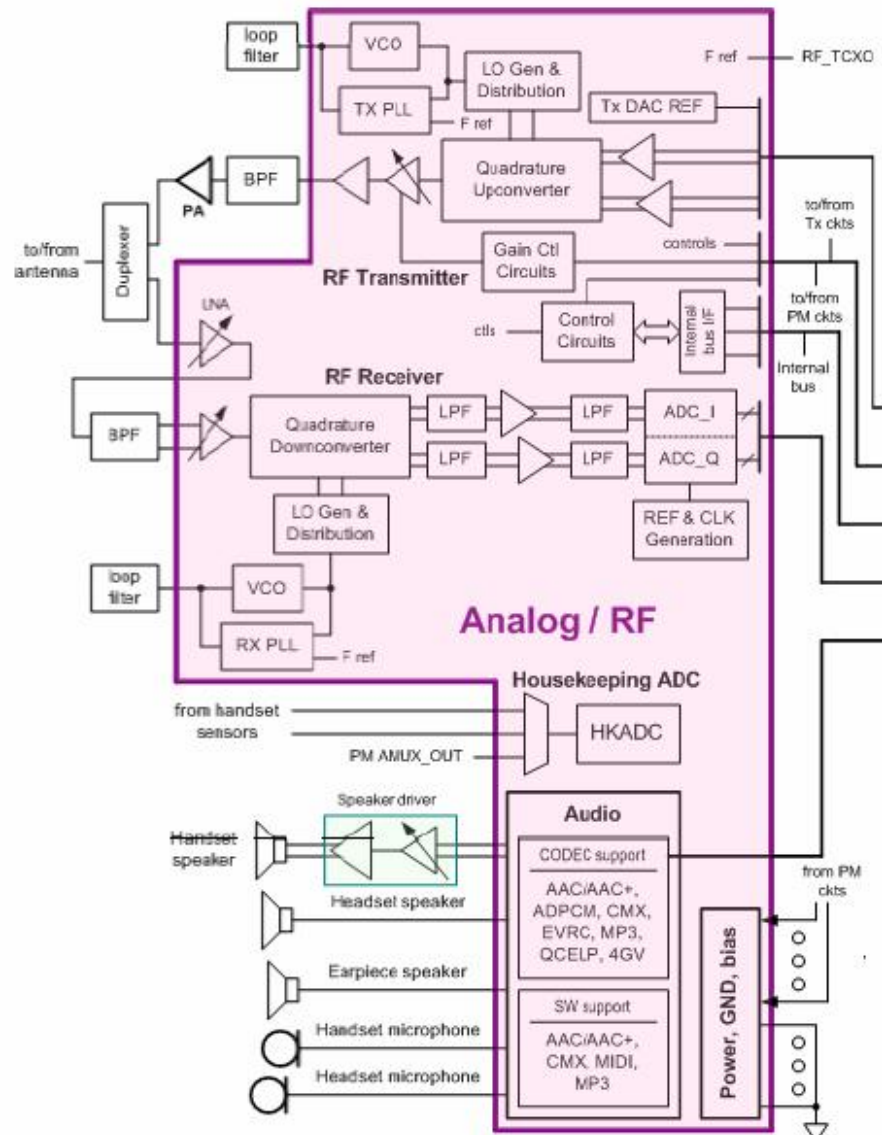
The C2900 has three clock sources: one is 19.2 MHz and the other two is 32 KHz. The diagram of the clock distribution is shown in the following figure. In the diagram, the clock of 19.2 MHz is the system work clock, which is generated by the crystal oscillator for the QSC6010. The clocks of the 32 KHz are respectively the sleep clock of the QSC6010 and work clock of the FM chip. When the phone is in the sleep status, the 19.2 MHz clock does not work. The clock required by the system is provided by the 32 KHz clock.

Figure 2-4 Clock diagram



2.2.3 Radio Frequency Unit

Figure 2-5 Functional modules of the RF unit



The functions are provided by the following parts:

- ┌ RF front-end: including the duplexer (B7630) and antenna matching circuits.
- ┌ Power amplification module: including 3*3 PA and AWT6307R.
- ┌ Other inactive parts: including SAW(Murata SAFEB836MAL0F00, Epcos B7838).

The antenna receives and transmits front-end RF signals.

The duplexer connected with the antenna splits receiving signals and transmission signals. The public end of the duplexer, which connects with the antenna, receives signals and outputs them through Rx. The public end inputs transmission signals through Tx and outputs them to the antenna. To avoid transmission signals from interfering receiving signals and ensure sensitivity, Rx of the duplexer is isolated from Tx,

The Transmit Signal Path of the QSC6010 RF Transceiver

The RF transmitter is based upon the RFT6122 IC design, but improved to include the latest innovations. The location of the RX PLL is changed to be in the RF receiver instead of in the RF transmitter. The transmitter provides the zero-IF signal channel, which supports the band within the CDMA2000 standard, BC0 (824–849 MHz) and BC3 (887–925 MHz). The transmit signal path includes baseband amplifiers, quadrature upconversion, gain control RF amplification, and an output driver amplifier.

Sophisticated Tx LO circuits implement the frequency plan and are completely integrated except for the loop filter (one resistor and two capacitors). All transmit LO signals are generated by the on-chip VCO under control of its PLL.

The Receive Signal Path of the QSC6010 RF Transceiver

The RF receiver is based upon the RFR6122 IC design, but includes significant innovative improvements. This zero-IF receive signal path also supports the BC0 and BC3 (Rx bands of 869 to 894 MHz and 832 to 870 MHz). The receive signal path includes the LNA, quadrature downconverter, analog baseband filters and buffers, and analog-to-digital converters (ADCs).

The incoming cellular-CDMA signal is routed from the antenna to the receiver path through the duplexer. The analog baseband output is delivered to the baseband circuits that also provide status and control signaling. Power reduction features (such as selective circuit power-off, gain control and bias control) extend standby time of the phone.

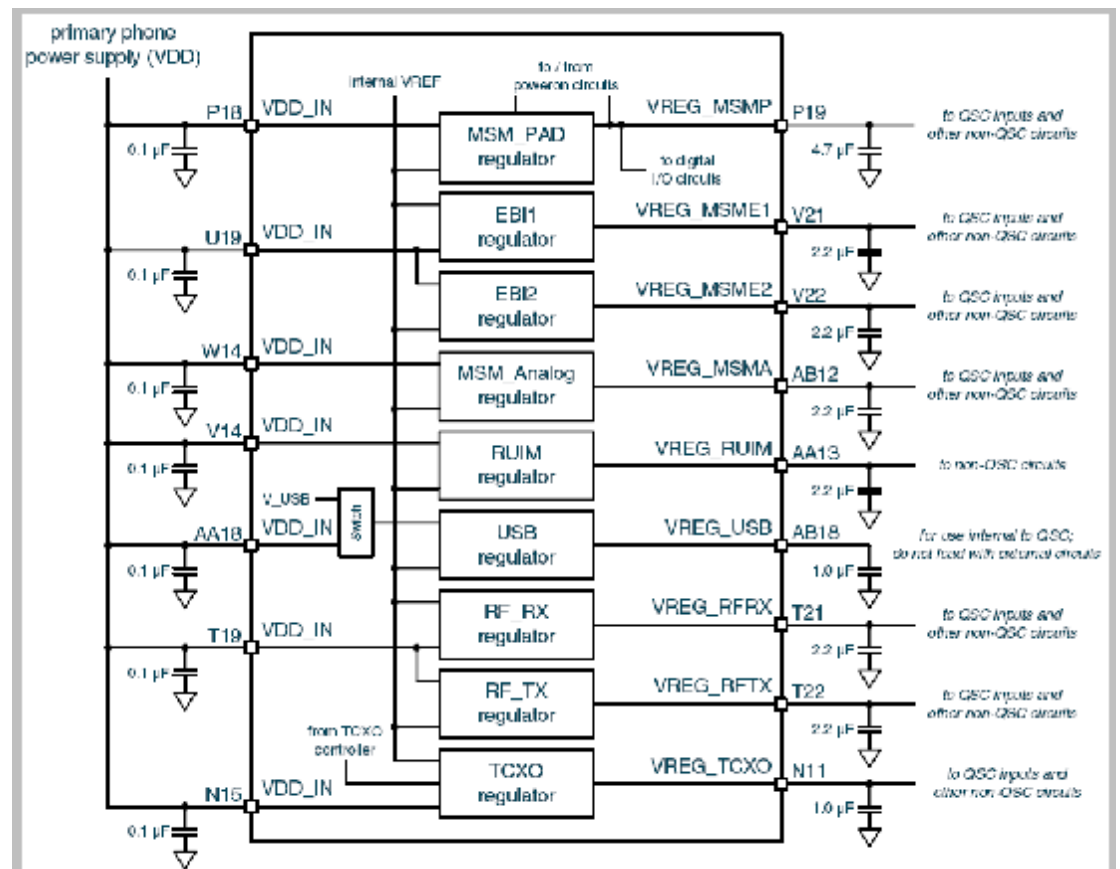
Like the Tx LO, all Rx LO circuits are completely integrated except for the loop filter (one resistor and two capacitors). All receive LO signals are generated by the on-chip VCO under control of its PLL. Since the zero-IF mode is sensitive to the LO compromise, it is internal to make $F_{VCO} \neq F_{LO} = F_{RF}$. The frequency of VCO output is converted to the frequency required by LO.

2.2.4 Power Supply/Reset/Charge Management

The QSC6010 integrates all the power management, general housekeeping, and user interface support functions of the phone into a single IC. According to the functions, the power management portion of the QSC6010 includes five modules: Input Power Management, Output Voltage Regulation, General Housekeeping, User Interfaces and PM Interfaces.

Power Management Solution

The QSC6010 includes all regulated voltage needed for most phones. Independent regulated power sources are required for various phone functions to avoid signal corruption between diverse circuits. It also supports power management sequencing to meet different requirements on voltage. Seven voltage regulators use the LDO circuits are provided, which are all programmable, and derived from a common reference circuit.

Figure 2-6 Block diagram of main output voltage interface**Table 2-1** Parameters of the output voltage interface of the power management module

Signal	Default voltage	Voltage range	Maximum current	Default status	Meaning
VREG_MSMC	1.3V	0.75–3.05	300 mA	On	Power the QSC6010 core.
VREG_MSMP	2.6V	1.5–3.05	300 mA	On	Power the QSC6010 pins.
VREG_MSMA	2.6V	1.5–3.05	150 mA	On	Analog
VREG_MSME1	1.8V	0.75–3.05	150 mA	On	EBI1
VREG_MSME2	2.9V	0.75–3.05	150 mA	On	EBI2
VREG_RFRX	2.6V	1.5–3.05	150 mA	Off	RF receiver
VREG_RFTX	2.6V	1.5–3.05	150 mA	Off	RF transmitter
VREG_RUIM	2.85V	1.5–3.05	150 mA	Off	RUIM
VREG_TCXO	2.85V	1.5–3.05	50 mA	On	TCXO

Signal	Default voltage	Voltage range	Maximum current	Default status	Meaning
VREG_USB	3.3V	3.0–6.1	50 mA	Off	USB

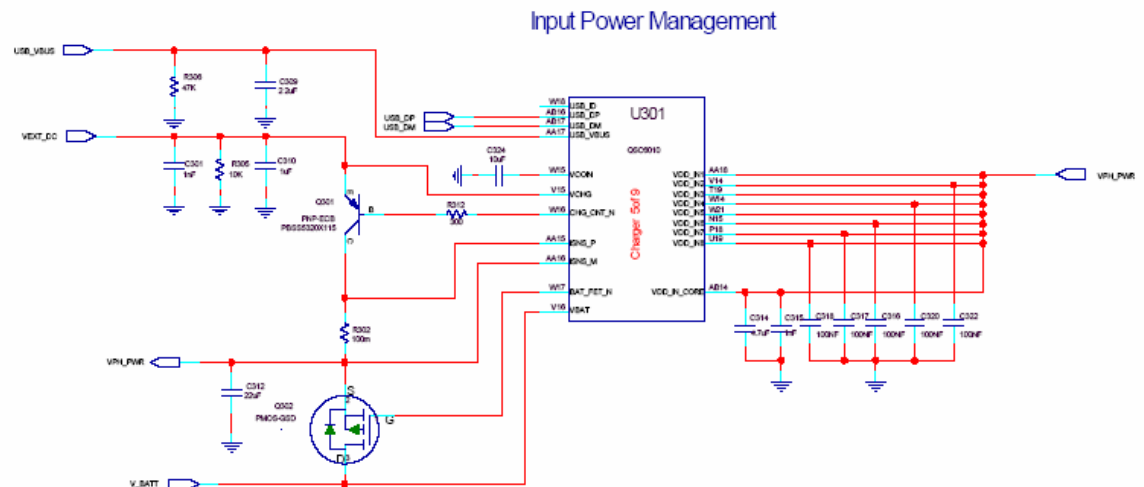
The QSC6010 is able to work in different modes. Currently, the C2900 controlled by the QSC6010 has the following three operating modes: work, dormant, and power-off.

Table 2-2 Power supply operating mode

Operating Mode	Valid Signals	Mode Description
Activate	Main battery or external power supply PS_HOLD = HIGH	QSC6010 works in the normal mode. MSMC, MSMP, MSMA, RFRX, RFTX, MSME2, MSME1, and TCXO are valid. Crystal oscillator is valid. TXCO buffer is on. Other functions and rectifier are controlled by SBI.
Dormant	Main battery or external power supply Turn off most QSC6010 functional circuits. PS_HOLD = HIGH	QSC6010 works in the power-saving mode. MSMC, MSMA, MSME2, MSME1, and MSMP are valid. Crystal oscillator is valid. TXCO buffer is on. Other functions and rectifier are turned off by the internal bus to reduce power consumption.
Power-off	The main battery works. PS_HOLD = LOW RTC_OSCDIS = LOW	Components are powered off and powered by the main battery. Crystal oscillator does not work. Other functions and rectifier are turned off.

Charging process

The charging process of the C2900 consists of three steps: constant current charging, constant voltage charging, or pulsed charging.

Figure 2-7 Block diagram of the charging circuit

I Charger power check

The circuit works with PM.

PM monitors charger voltage (Pin V15, VCHG) and board main power B+ voltage (Pin AA15, ISNS_M). The connection of the charger is defined and the status of the charger voltage is by comparing the two voltages (the hysteresis range is set for threshold).

PM detects the charger to select an input mode and switch between the two modes (charger or main battery). If $V(VCHG) > V(B+)$, the charger voltage is greater than the battery voltage and the pass transistor is enabled. Then phone is charged by the charger. If $V(VCHG) \leq V(B+)$, the battery voltage is higher than the charger voltage and the pass transistor is disabled. Then phone is powered by the battery. To forbid the phone to automatically switch to use the charger power, configure through the software. VCHG is grounded by connecting in parallel with a 10 k resistance and a 1 μ f capacitor. If the charger is not connected with the phone, the resistance can pull VCHG to 0 V to make sure that the charger is detected as not connected. The parallel-connected capacitor protects EMC, provides linear filter, and ensures circuit stability.

The phone is powered by the main battery

QSC6010 charging process consists of three steps: trickle charging, constant current charging, and constant voltage charging. If a battery is almost discharged, charge it from trickle charging to control the current and avoid the main power supply B+ is lowered. After the minimal voltage is set up through trickle charging, the software enables the constant current charging mode to fast charge the battery. Constant current charging is also called fast charging. Once the Li-ion battery reaches the target voltage, the charger can switch to the constant voltage charging.

- I Constant current charging: Pass transistor is enabled and charging current is from the charger. The charger limits the current (to lower the internal heat of the phone). The HKADC of QSC6010 detects the battery voltage that is measured when the pass transistor is on. If the preset target voltage is reached (it is set as VBATDET threshold, slightly higher than VBSpec in convenience for fast charging), the charging current is decreased and the constant current charging ends.

- I Constant voltage charging: In this process, compare the main power B+ (roughly equal to the battery voltage) with VMAXSEL (it is set through the SBI on the software; The charging limit voltage is always set as 4.2 V according to the battery specifications) to regulate the base current. Try to make value of B+ is similar to that of VMAXSEL (that is the constant voltage). The smaller difference between the values of the battery voltage and B+, the smaller the current is. When the battery voltage is equal to the threshold set in the software (the battery voltage is measured by disconnecting the pass transistor). Then charge with the constant voltage for another period (that means keeping the charging status; the duration is subject to the software). Then, stop charging.

Backup battery

The backup battery is charged by the battery through the software. The existing 1 μ F capacitor can realize SMPL function only.

UVLO

Under-voltage lockout: The UVLO continuously monitors the handset main power (VPH_PWR) voltage. Once the voltage is lower than the threshold, PM automatically turns off.

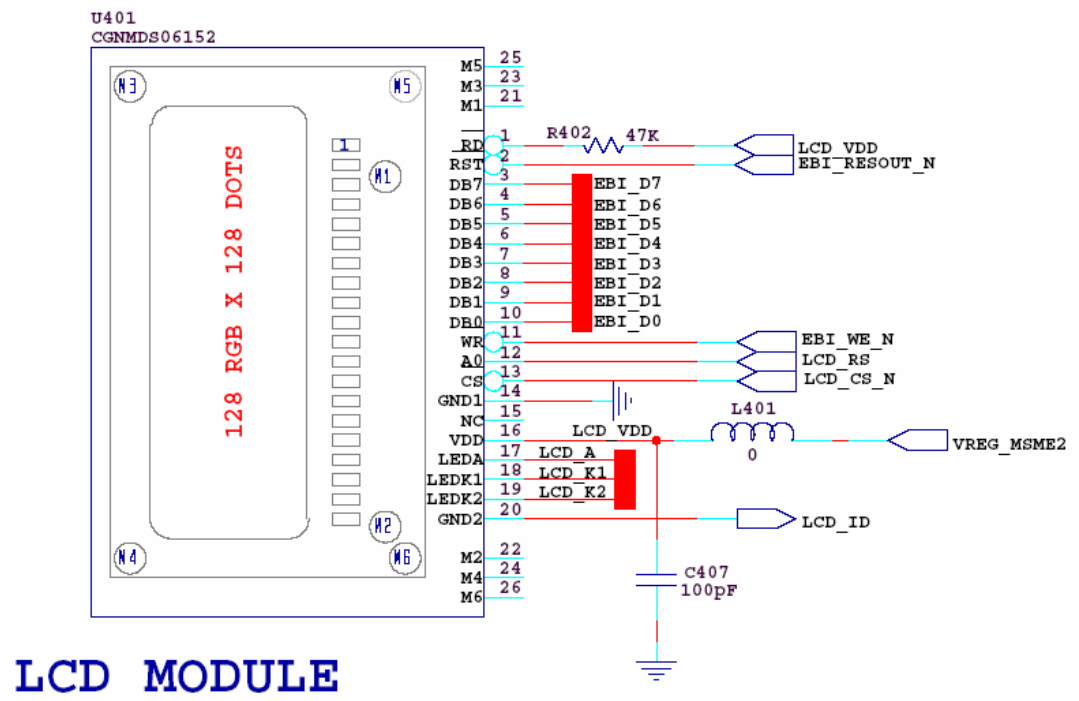
UVLO is the pure hardware function. Parameter software cannot be controlled. Before UVLO, no interruption occurs. PON_RESETB is driven LOW to report to QSC6010. Specifications of PM UVLO are as follows:

Parameter	Comments	Min	Typ	Max	Unit	Notes
Threshold voltage	Falling, leaving valid range	2.423	2.55	2.678	V	
Hysteresis		120	165	210	mV	
UVLO detection interval			1.0		μ sec	

2.2.5 Peripheral Circuit

LCD

The C2900 is equipped with the 128 $\times$ 128 pixel CSTN LCM with two built-in high brightness white LEDs. The recommended typical current value is 20 mA. It is driven by the embedded current source of QSC6010. LCM driver chip adopts S6B33BG. Enable the 8080 series 8bit parallel mode for C2900. Figure 2-8 shows the circuit working principle.

Figure 2-8 LCD interface circuit**Table 2-3** LCD pin descriptions

Pin No.	Signal name	Direction	Function	Remark
1	/RD	O	Data input enabling	It is valid when the level is low.
2	/RESET	I	Power-on reset signal	It is valid when the level is low.
3	DB7	I/O	Concurrent data interface	—
4	DB6	I/O	Concurrent data interface	—
5	DB5	I/O	Concurrent data interface	—
6	DB4	I/O	Concurrent data interface	—
7	DB3	I/O	Concurrent data interface	—
8	DB2	I/O	Concurrent data interface	—
9	DB1	I/O	Concurrent data interface	—
10	DB0	I/O	Concurrent data interface	—
11	/WR	I	Read and write control signals	† High level: read signals † Low level: write

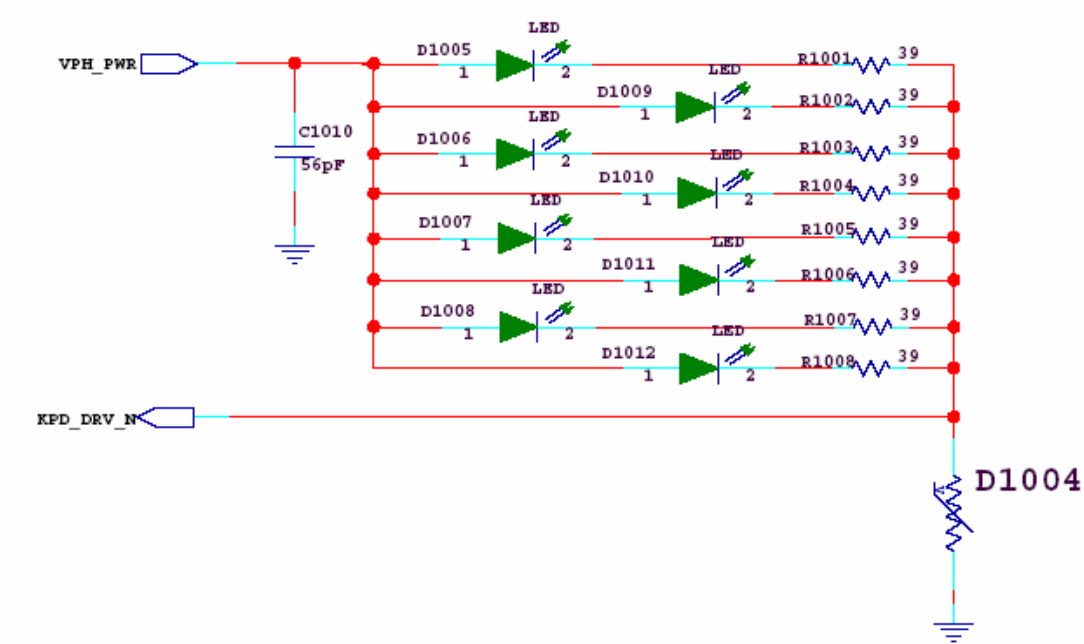
Pin No.	Signal name	Direction	Function	Remark
12	RS	I	LCD data and control signals	
13	/CS	I	LCD bus enabling	It is valid when the level is low.
14	GND	GND	GND	—
15	NC	—	None	—
16	VDD	POWER	Power supply	—
17	LEDA	I	Backlight control	—
18	LEDK1	O	Backlight control	—
19	LEDK1	O	Backlight control	—
20	LCD-ID	O	ID identity	—

Key LED

The C2900 implements a keypad LED and a LCD backlight LED.

Figure 2-9 shows the LED interface circuits. The keypad LED uses eight blue lights. If each light is led through, the voltage is decreased to 2.80 V. If the battery voltage is 4.2 V, the current for each light is 7 mA; if the battery voltage is 3.5 V, the current for each light is 3.5 mA. Adjust the series resistance to control the actual current for each light. To balance the brightness and the power consumption, set a suitable series resistance. Control the QSC6010 power management module to set keypad LED.

Figure 2-9 Keypad LED interface circuit



Keypad

Figure 2-10 Keypad interface circuit

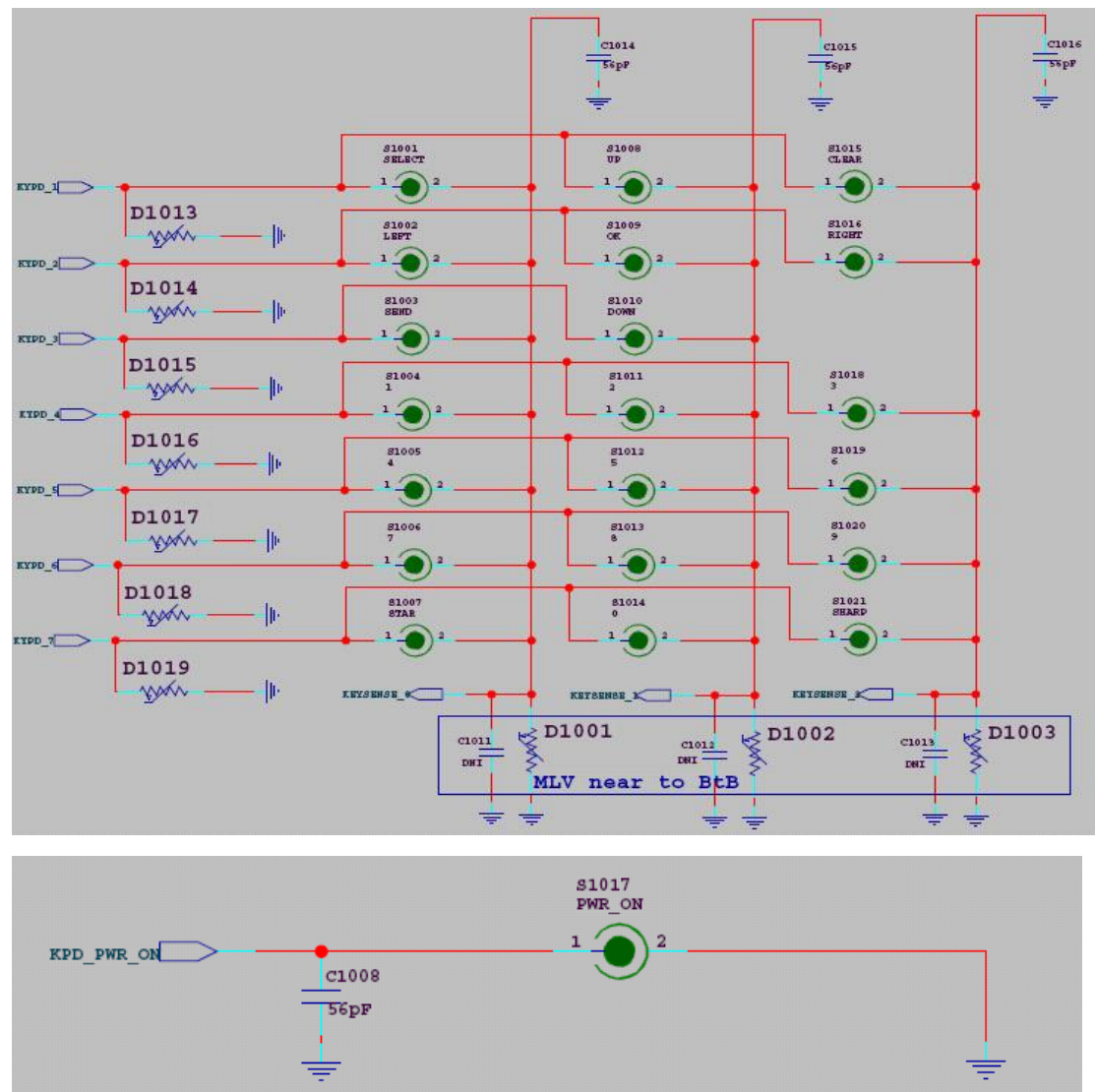


Table 2-4 Keypad pin definition

No.	Signal	Direction	Function	Remark
1	KYPD_1	I	Keypad line scan signal 1	—
2	KYPD_2	I	Keypad line scan signal 2	—
3	KYPD_3	I	Keypad line scan signal 3	—
4	KYPD_4	I	Keypad line scan signal 4	—
5	KYPD_5	I	Keypad line scan signal 5	—
6	KYPD_6	I	Keypad line scan signal 6	—

No.	Signal	Direction	Function	Remark
7	KYPD_7	I	Keypad line scan signal 7	–
8	KEYSENSE_0	O	Keypad column scan signal 0	–
9	KEYSENSE_1	O	Keypad column scan signal 1	–
10	KEYSENSE_2	O	Keypad column scan signal 2	–
11	KPD_PWR_ON	I	Scan completion and power switch signal	–

KPD_PWR_ON scans the PWR_ON key. Connect signals directly to the control switch of the power management module. When the handset is powered off, press the PWR_ON key to trigger the power-on sequence of the power management module until the whole system starts normally. When the handset is working normally, press the PWR_ON key. Then KPD_PWR_ON receives key trigger signals and sends them to the CPU for processing.

Audio Processing

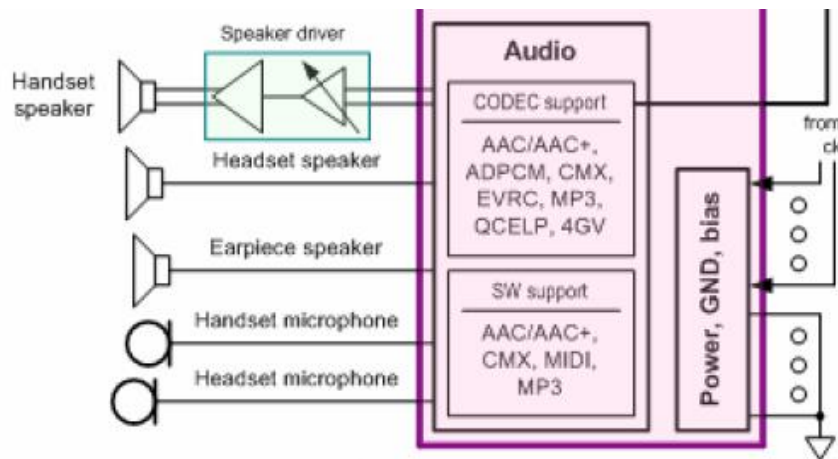
The audio module of the C2900 consists of QSC6010 audio part, audio power amplifier, speaker, receiver, microphone, earpiece, and QSC6010 power supply.

The C2900 provides three kinds of audio output:

- ┌ Receiver output: The receiver locates at the front side of the C2900 receives signals from EAR1O_P/EAR1O_N of QSC6010, and voice in the normal mode.
- ┌ Speaker output: AUXOP/AUXON of QSC6010 outputs audio signals. Audio signals are amplified by a built-in audio amplify circuit and sent to the receiver for polyphonic ringtone and handsfree audio.
- ┌ Earpiece output: The C2900 is compatible with stereo audio channel and stereo audio channel. The earpiece is realized through IO.

Vibration and loudspeaker

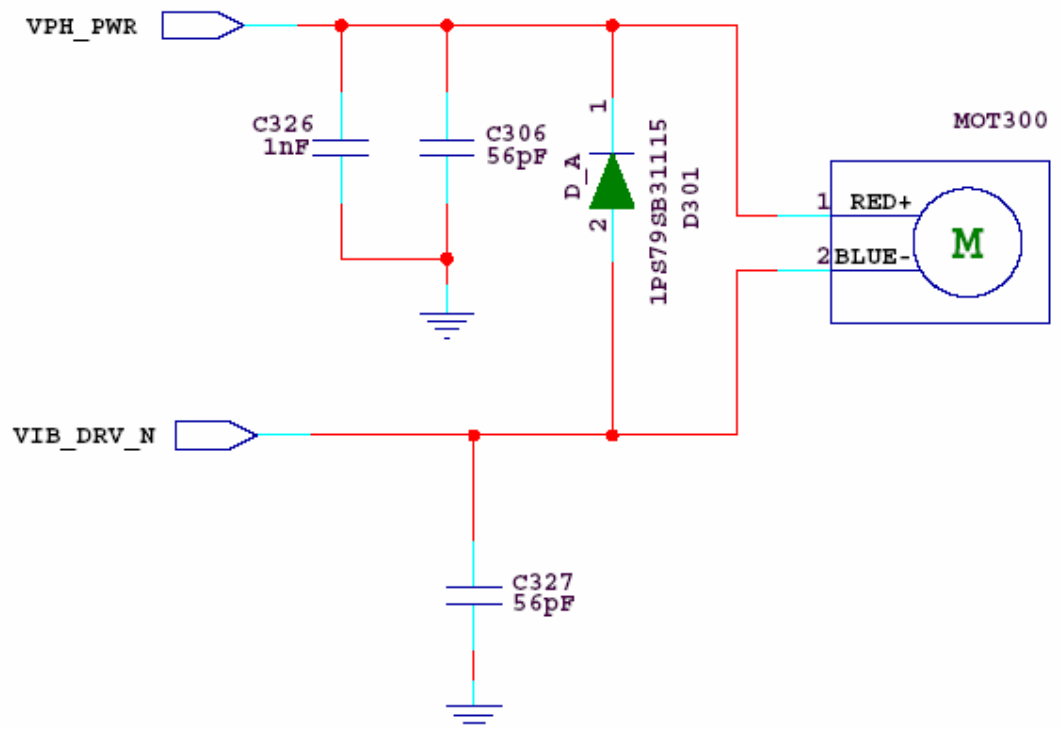
Since loudspeaker requires a higher output power, audio amplifier is used. The C2900 is equipped with a speaker of 8 Ω as an audio output device.

Figure 2-11 Audio receiver and transmitter circuit

Vibrator

The vibrator is powered directly by battery voltage, using the built-in driver of the QSC6010. The two ends of the vibrator connect reverse diode to restrain reverse electromotive force. The vibrator connects in parallel with a 56 pF capacitor to restrain the outgoing of in-board high-frequency noise. QSC6010 VIB_DRV_N is the driver pin for the vibrator.

See Figure 2-12.

Figure 2-12 Vibrator interface circuit

UIM Card Slot

The C2900 supports R_UIM. It connects the R_UIM card through the UIM card slot. Figure 2-13 shows the R_UIM card slot. QSC6010 provides the R_UIM card slot with VREG_RUIM power of 2.85 V. Reset signals, clock signals, and data signals of the R_UIM card slot can seamlessly connect with the main chipset.

Figure 2-13 UIM card interface

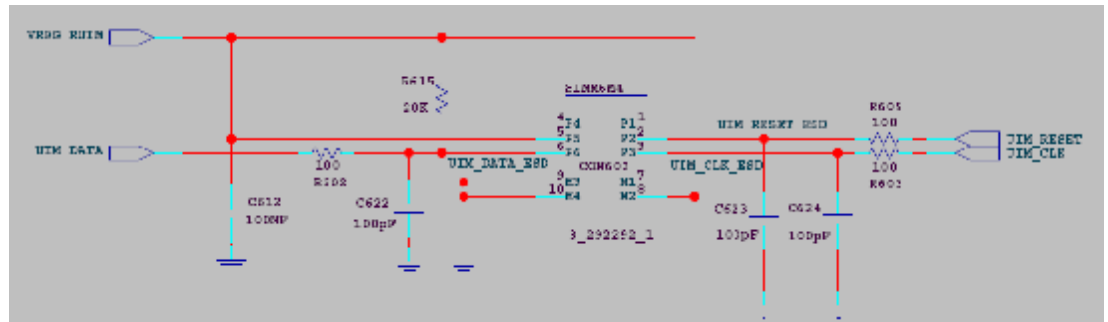


Table 2-5 UIM card slot signals

Pin No.	Pin name	IO Direction	Description
1	GND		Ground
2	VREG_RUIM	Input	UIM card power supply
3	UIM_DATA	Bi-directional	UIM card data signal
5	VREG_RUIM	Input	UIM card power supply
6	UIM_RST	Input	UIM card reset signal
7	UIM_CLK	Input	UIM card clock signal

External IO interface

Figure 2-14 Functional block diagram of the external IO interface circuit

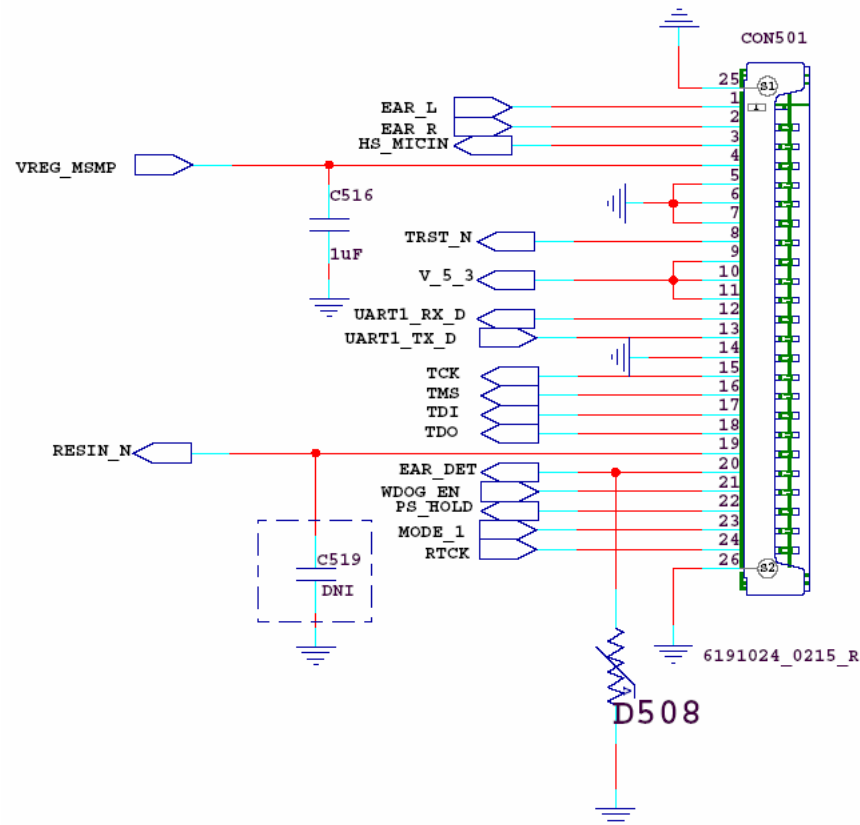


Figure 2-14 shows the external IO interface circuit. The IO connector, at the bottom of the C2900 adopts 24-PIN, providing data, debug, earpiece, and charger connectors.

Table 2-6 IO pins

Pin No.	Latest recommendation	
	Pin name	Description
1	EAROL	Detection of the earpiece output left audio channel/mono audio channel
2	EAROR	Earpiece output right audio channel/mono audio channel
3	MICIN	Earpiece MIC input
4	VREG_MSMP	Baseband chip PAD power voltage output
5	CGND	Charger ground
6	CGND	Charger ground
7	CGND	Charger ground

Pin No.	Latest recommendation	
	Pin name	Description
8	TRST_N	JTAG reset signal
9	VCHG	Charger power input
10	VCHG	Charger power input
11	VCHG	Charger power input
12	S_RX	Serial port input
13	S_TX	Serial port output
14	SGND	Serial port ground, earpiece ground
15	TCK	JTAG clock input
16	TMS	JTAG mode selection
17	TDI	JTAG data input
18	TDO	JTAG data output
19	RESIN_N	Board reset input
20	Ear_Detect	Detection of inserting the earpiece (stereo audio channel)
21	WDOG_EN	Dongle enabling signal
22	PS_HOLD	Power-on holding signal
23	MODE_1	CPU mode control signals
24	RTCK	JTAG synchronize clock output

FM Circuit

The built-in FM radio of the C2900 adopts the EA5767HN chip of PHILIPS to receive and process the FM signals. The output stereo audio signals are output to the earpiece after they are amplified by LM4811.

The TEA5767HN includes the modulation module, receiver and mixer, demodulator, MPX decoder, and I²C interface. When the chip works, the required frequency is sent to the selective module through the I²C interface. The mixing circuit mixes the received specified frequency (76 MHz–108 MHz) into intermediate frequency (225 KHz). Then the audio is output through the process of the IF filter, demodulator, and decoder.

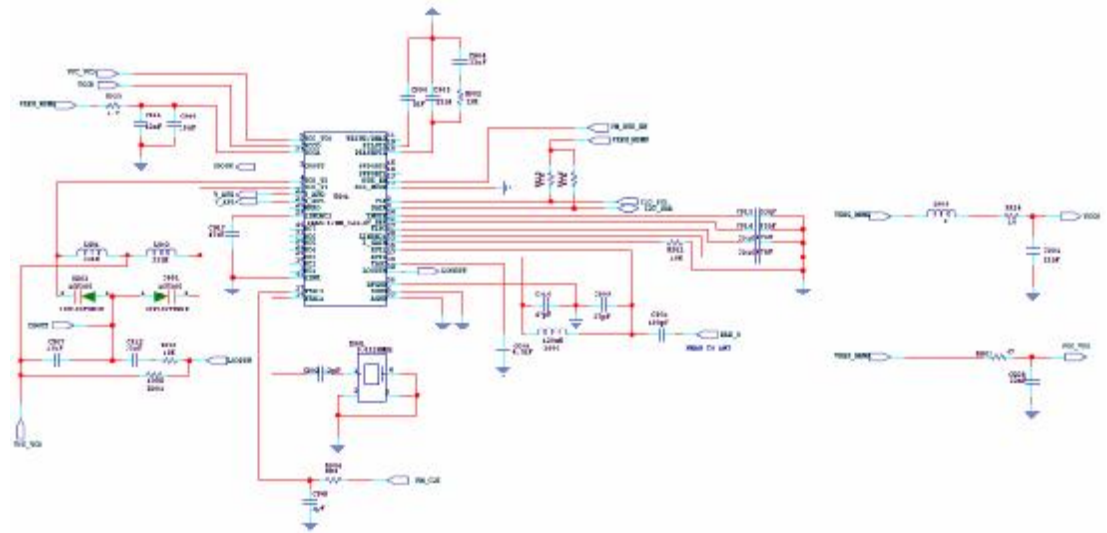
The I²C interface control uses the I²C interface of QSC6010. The following table lists the pin assignment.

Table 2-7 QSC6010 I2C pin assignment

Net List	QSC6010 PIN assignment	Description
S_CLK	GPIO19	I ² C clock line
S_DAT	GPIO18	I ² C data line

FM uses the earpiece as the antenna. Before listening to FM, connect the earpiece to the handset. To avoid interference between FM and RF, the FM module is placed in a shielding box.

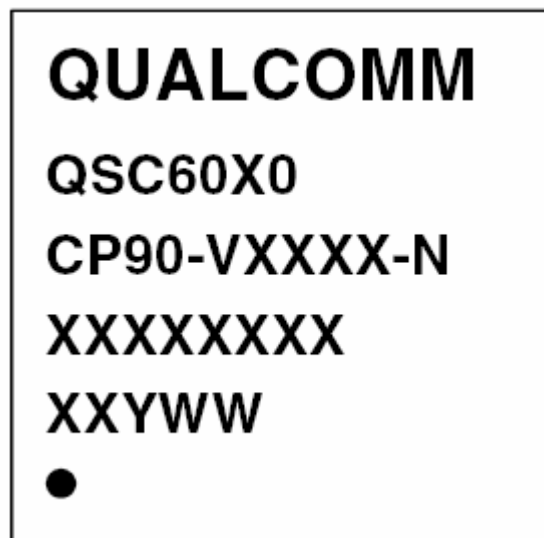
The two varactor of VCO are outside the chip. Note the parasitic capacitor of PCB. Use inductance of 820 nH for antenna and ground. At 97 MHz, the resistance is 499 Ω , which is greatly higher than the input resistance of FM antenna (40 Ω).

Figure 2-15 FM conceptual diagram

3 Functional Chip

3.1 Core Chipset

The baseband processing sub-system of MSM6000 includes audio CODEC unit, baseband signal processing unit, and CPU of protocol software running. All the functional units are integrated in the MSM6000.



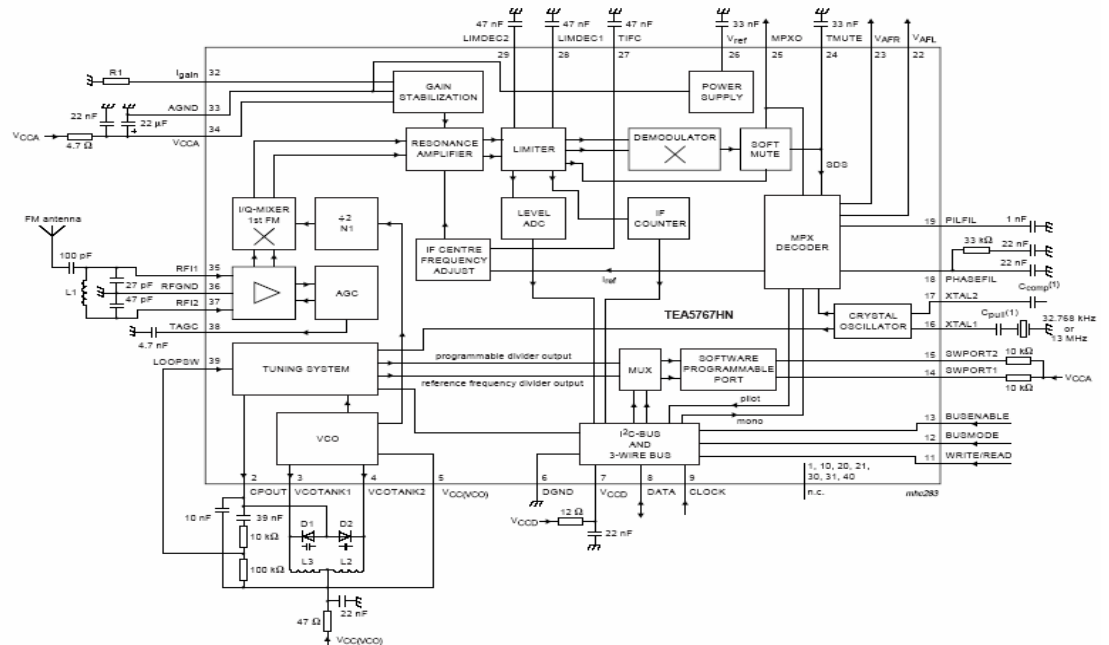
Line	Marking	Description
1	QUALCOMM	QUALCOMM name or logo
2	QSC60X0	QUALCOMM product name QSC6010 (low tier) QSC6020 (mid tier) QSC6030 (high tier)
3	CP90-VXXXX-N	QUALCOMM MCN number CP90-V9690-N: QSC6010 CP90-V0260-N: QSC6020 CP90-V0261-N: QSC6030 N = version number
4	XXXXXXXXXX	XXXXXXXXXX = manufacturer information
5	XXYWW	XX = manufacturing information Y = single digit year code WW = week code
6	dot	pin 1 indicator

3.2 FM Chip

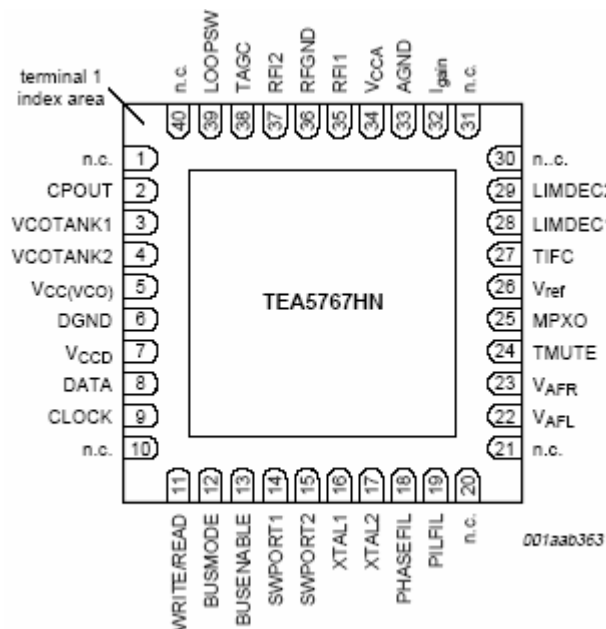
The FM chip adopts the TEA5767HN of Philips. The TEA5767HN is a single-chip, electronic tuning stereo FM radio. With rounded IF selections and demodulations, it is often used for occasions of low consumption. TEA5767HN can adjust the wireless communications automatically, requiring only few external components with low power consumption. It is suitable for the FM frequency band in European, North American and Japan.

Chip Functional Block Diagram

Figure 3-1 TEA5767HN functional block diagram



Configuration Diagram of the Chip Pins



Chip PIN Functions

Table 3-1 TEA5767HN PIN functions.

Symbol	PIN	Description
n.c.	1	Disconnected
CPOUT	2	Integrate CP output of PLL.
VCOTANK1	3	VCO adjusts the circuit output 1.
VCOTANK2	4	VCO adjusts the circuit output 2.
V _{CC(VCO)}	5	VCO voltage
DGND	6	Digit ground
V _{CCD}	7	Digital voltage
DATA	8	Input/output of the data line of the bus
CLOCK	9	Input of the clock line of the bus
n.c.	10	Disconnected
WRITE/READ	11	3-wire bus read/write control input
BUSMODE	12	Input of bus mode selection
BUSENABLE	13	Bus enabling input
SWPORT1	14	Software programming port 1
SWPORT2	15	Software programming port 2
XTAL1	16	Crystal oscillator input 1
XTAL2	17	Crystal oscillator input 2
PHASEFIL	18	Phase discrimination filter
PILFIL	19	Low pass filter
n.c.	20, 21	Disconnected
V _{AFL}	22	Left audio output voltage
V _{AFR}	23	Right audio output voltage
TMUTE	24	Time constant of the soft mute
MPXO	25	MPX signal output of FM demodulator
V _{ref}	26	Reference voltage

Symbol	PIN	Description
TIFC	27	Time constant adjusted by the IF center
LIMDEC1	28	IF decoupling limiter 1
LIMDEC2.	29	IF decoupling limiter 2
n.c.	30,31	Disconnected
I _{gain}	32	Gain control current of the IF filter
AGND	33	Analog ground
V _{CCA}	34	Analog voltage
RFI1	35	RF input 1
RFGND	36	RF ground
RFI2	37	RF input 2
TAGC	38	Time constant of the RF automatic gain control
LOOPSW	39	Integrated PLL filter on/off output
n.c.	40	Disconnected

Chip Parameter Descriptions

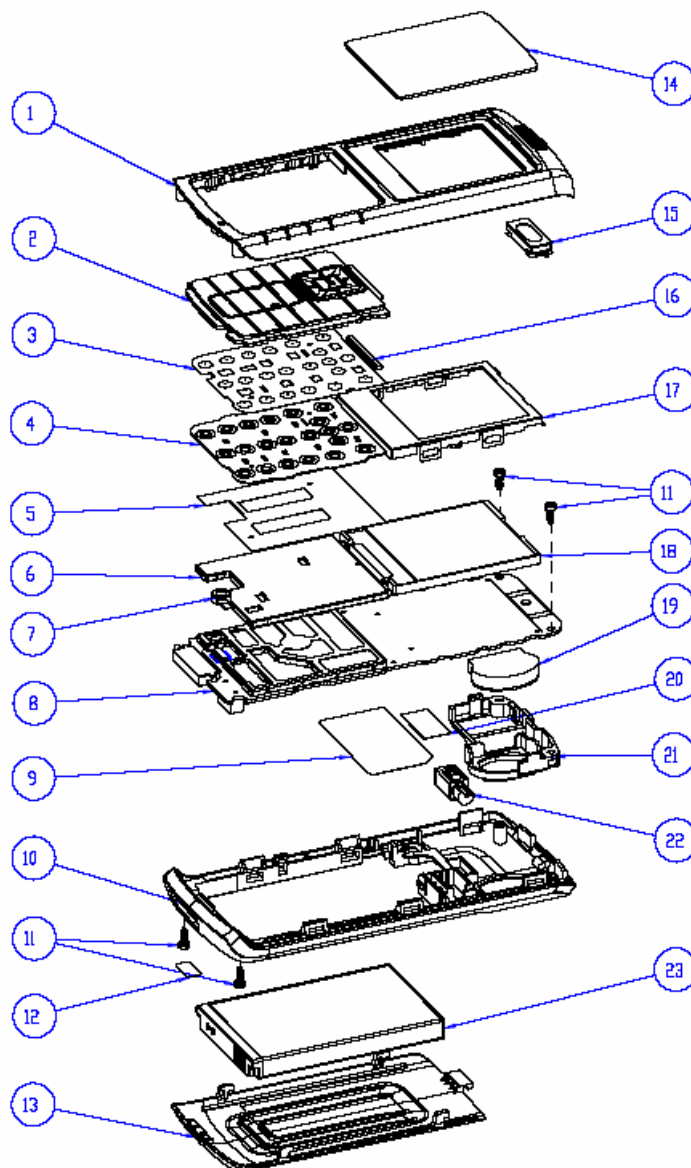
Table 3-2 Descriptions of FM chip parameters

Symbol	Parameter	Condition	MIN	TYP	MAX	UNIT
V _{CCA}	Analog voltage		2.5	3.0	5.0	V
V _{CC(VCO)}	VCO voltage		2.5	3.0	5.0	V
V _{CCD}	Digital voltage		2.5	3.0	5.0	V
I _{CCA}	Analog current	Working; VCCA = 3 V	6.0	8.4	10.5	mA
		Standby; VCCA = 3 V	–	3	6	μA
I _{CC(VCO)}	VCO voltage	Working; VVCOTANK1 = VVCOTANK2 = 3 V	560	750	940	μA
		Standby; VVCOTANK1 = VVCOTANK2 = 3 V	–	1	2	μA
I _{CCD}	Digital voltage	Working; VCCD = 3 V	2.1	3.0	3.9	mA

Symbol	Parameter	Condition	MIN	TYP	MAX	UNIT
		Standby; VCCD = 3 V				
		The enabling line of the bus is high.	30	56	80	μA
		The enabling line of the bus is low.	11	19	26	μA
$f_{\text{FM(ant)}}$	FM input frequency		76	–	108	MHz
T_{amb}	Peripheral temperature	VCCA = VCC(VCO) = VCCD = 2.5 V to 5 V	–10	–	+75	$^{\circ}\text{C}$
FM overall system parameters;						
V_{RF}	RF sensitivity input voltage	$f_{\text{RF}} = 76 \text{ MHz to } 108 \text{ MHz}; f = 22.5 \text{ kHz};$ $f_{\text{mod}} = 1 \text{ kHz}; (S+N)/N = 26 \text{ dB};$ de-emphasis = 75 μs ; L = R;	–	2	3.5	μA
$\tilde{S}_{200}$	Low side 200KHz selectivity	$f = 200 \text{ kHz}; f_{\text{RF}} = 76 \text{ MHz to } 108 \text{ MHz};$	32	36	–	dB
S_{+200}	High side 200KHz selectivity	$f = +200 \text{ kHz}; f_{\text{RF}} = 76 \text{ MHz to } 108 \text{ MHz};$	39	43	–	dB
$V_{\text{AFL}}; V_{\text{AFR}}$	Left and right audio output voltage	$V_{\text{RF}} = 1 \text{ mV}; L = R; f = 22.5 \text{ kHz}; f_{\text{mod}} = 1 \text{ kHz};$ de-emphasis = 75 μs	60	75	90	mV
(S+N)/N	maximum signal plus noise-to-noise ratio	$V_{\text{RF}} = 1 \text{ mV}; L = R; f = 22.5 \text{ kHz};$ $f_{\text{mod}} = 1 \text{ kHz};$ de-emphasis = 75 μs ; BAF = 300 Hz to 15 kHz	54	60	–	dB
cs(stereo)	Stereo channel spacing	$V_{\text{RF}} = 1 \text{ mV}; R = L = 0$ or $R = 0$ and $L = 1$ including 9 % pilot; $f = 75 \text{ kHz}; f_{\text{mod}} = 1 \text{ kHz};$ data byte 3 bit 3 = 0; data byte 4 bit 1 = 1	24	30	–	dB
THD	Total harmonic distortion	$V_{\text{RF}} = 1 \text{ mV}; L = R; f = 75 \text{ kHz}; f_{\text{mod}} = 1 \text{ kHz};$ de-emphasis = 75 μs	–	0.4	1	%

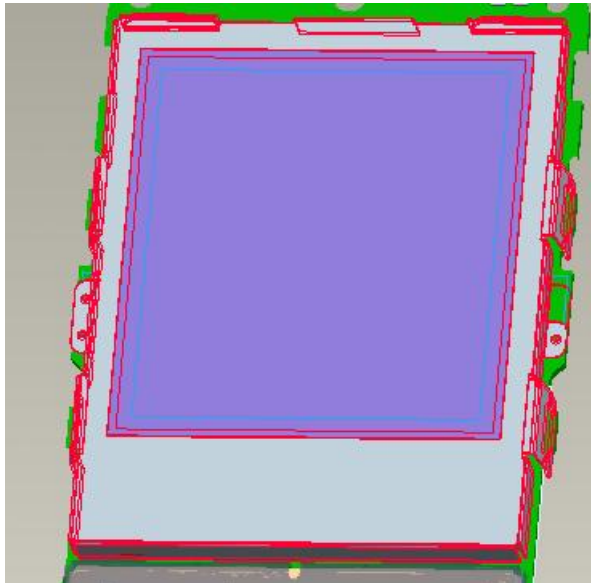
4 Assembling Description

4.1 C2900 Explosion Diagram

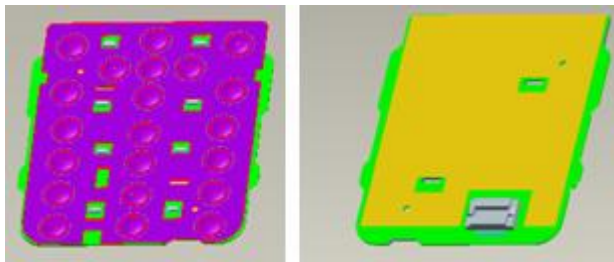


4.2 Assembling

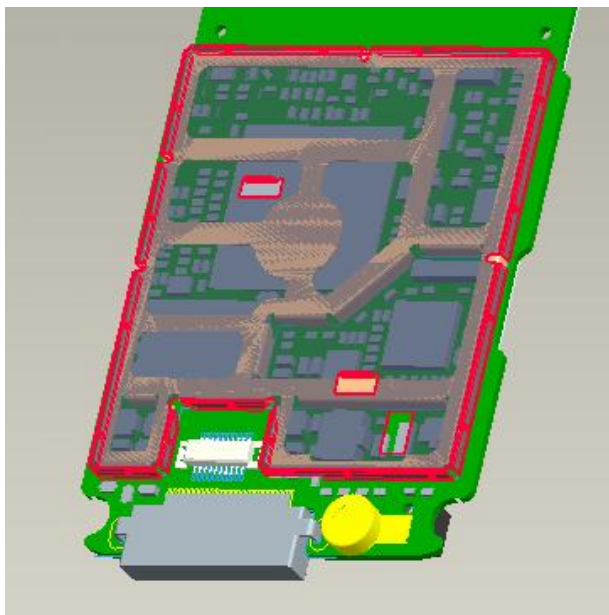
1. Assemble the LCD shielding case.



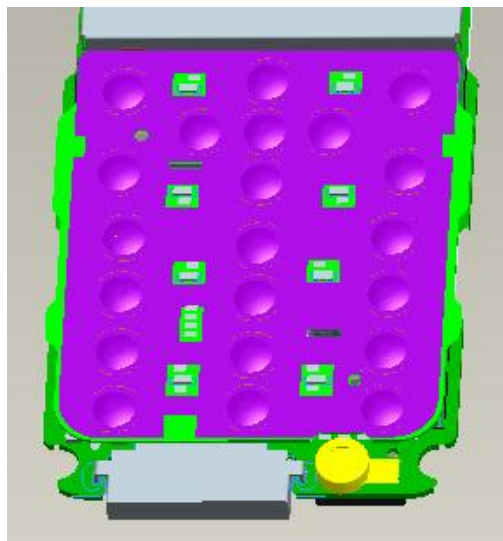
2. Paste the Metal Dome and double faced adhesive tape of the keypad.



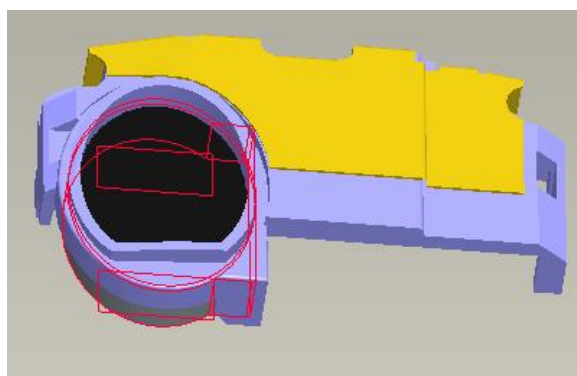
3. Install the baseband shielding cover.



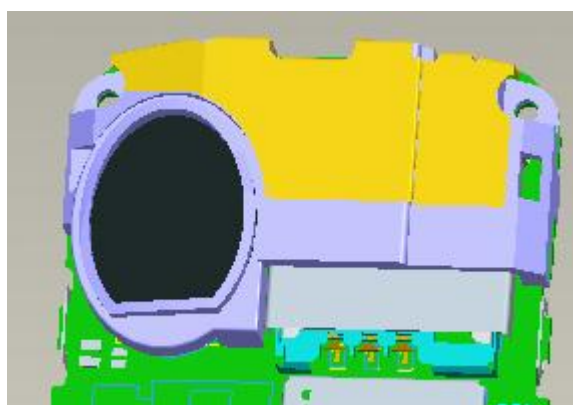
4. Install keypad board.



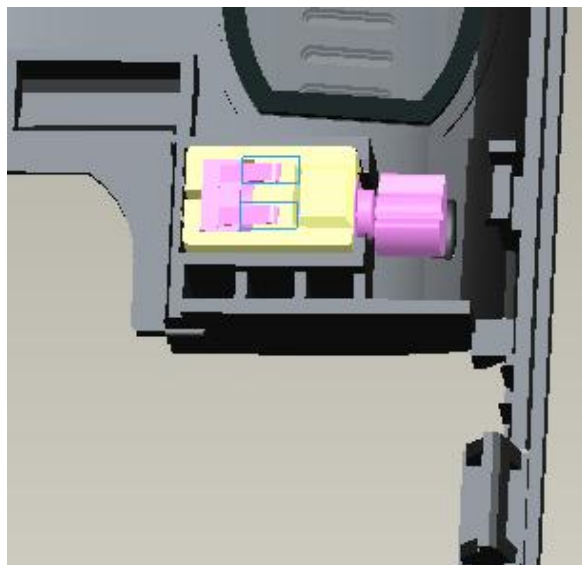
5. Assemble the speaker.



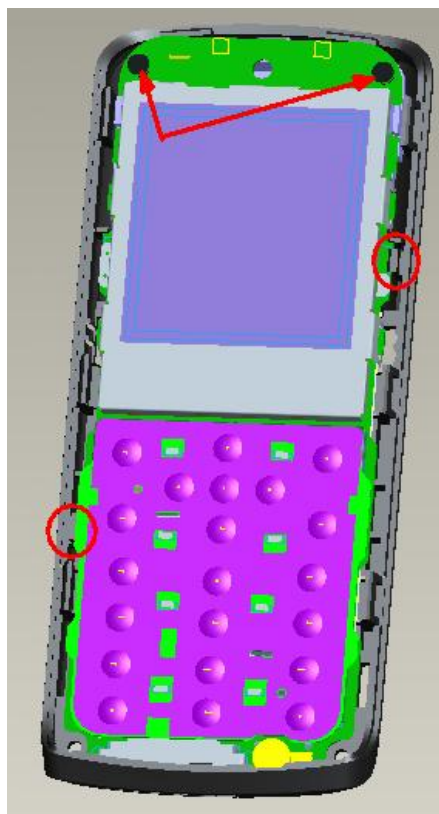
6. Assemble the antenna.



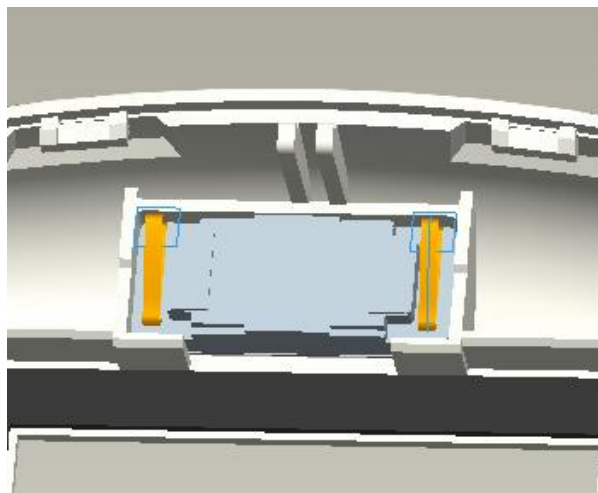
7. Install the motor at the back shell.



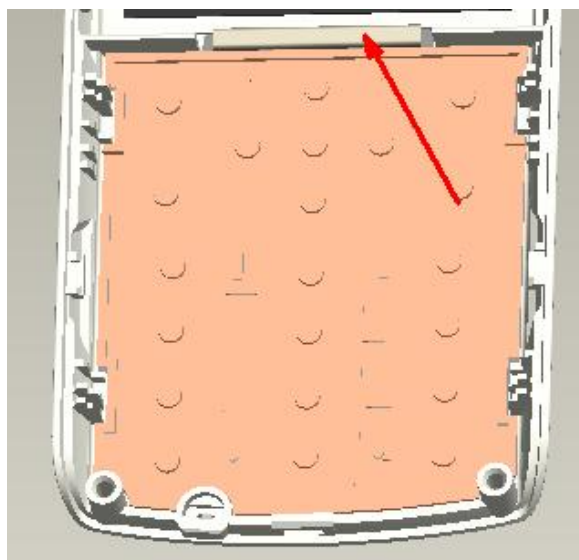
8. Install the main board at the back shell, and fix the two screws at the top.



9. Install the receiver.



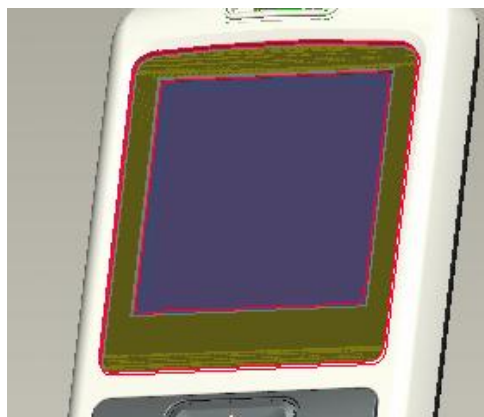
10. Assemble the keypad.



11. Close the front and the back cover, with fixing the two screws at the bottom.



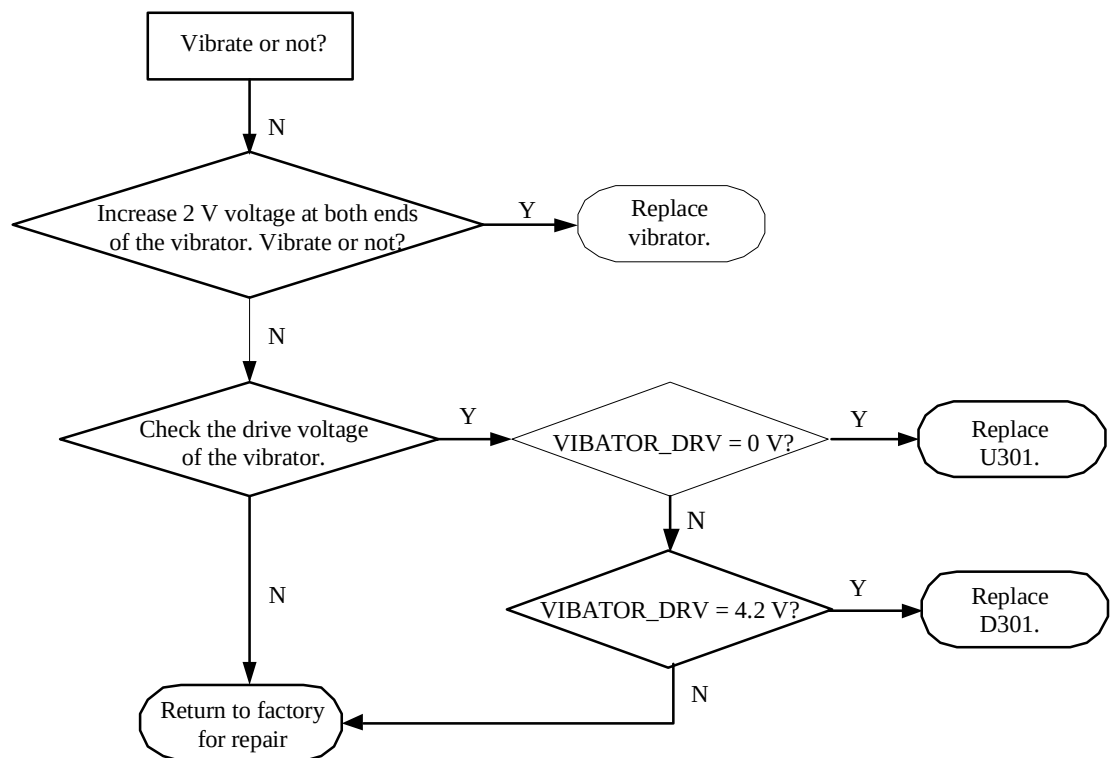
12. Paste the lens.



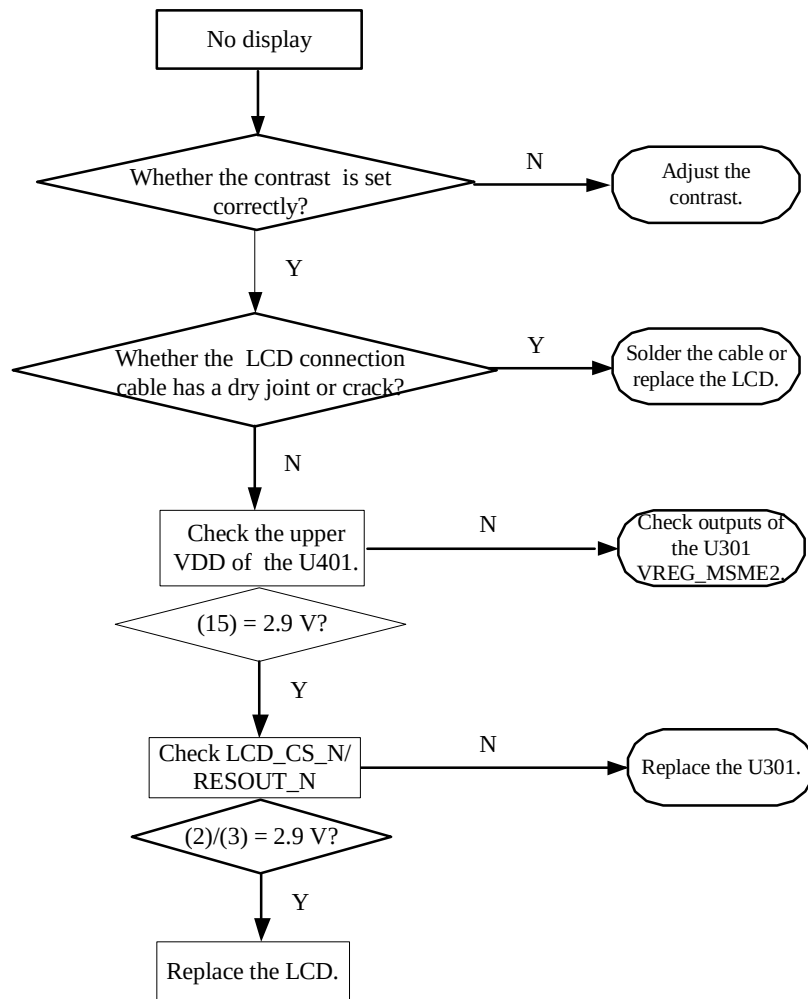
13. Install the battery and the battery cover.

5 Troubleshooting

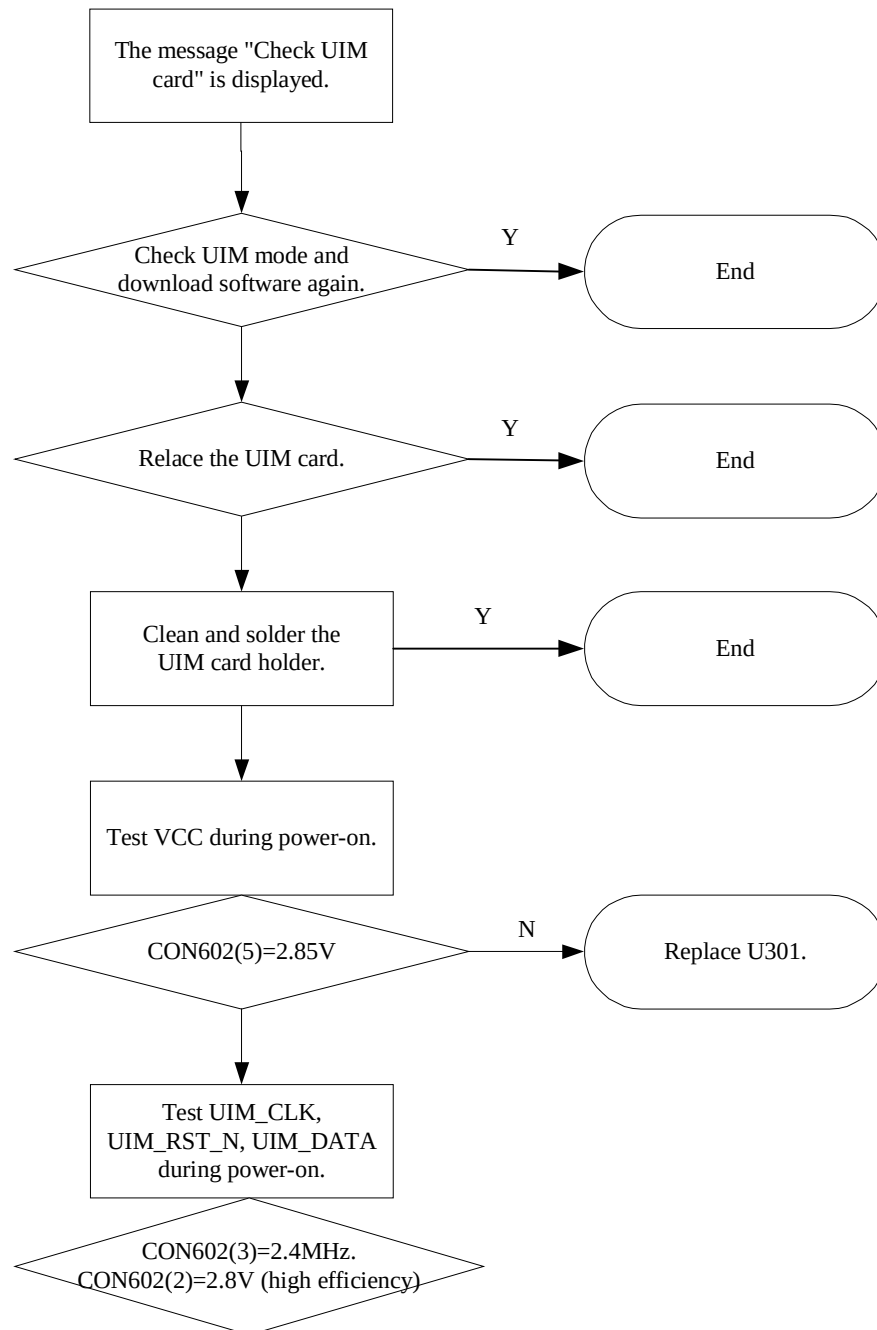
5.1 No Vibration



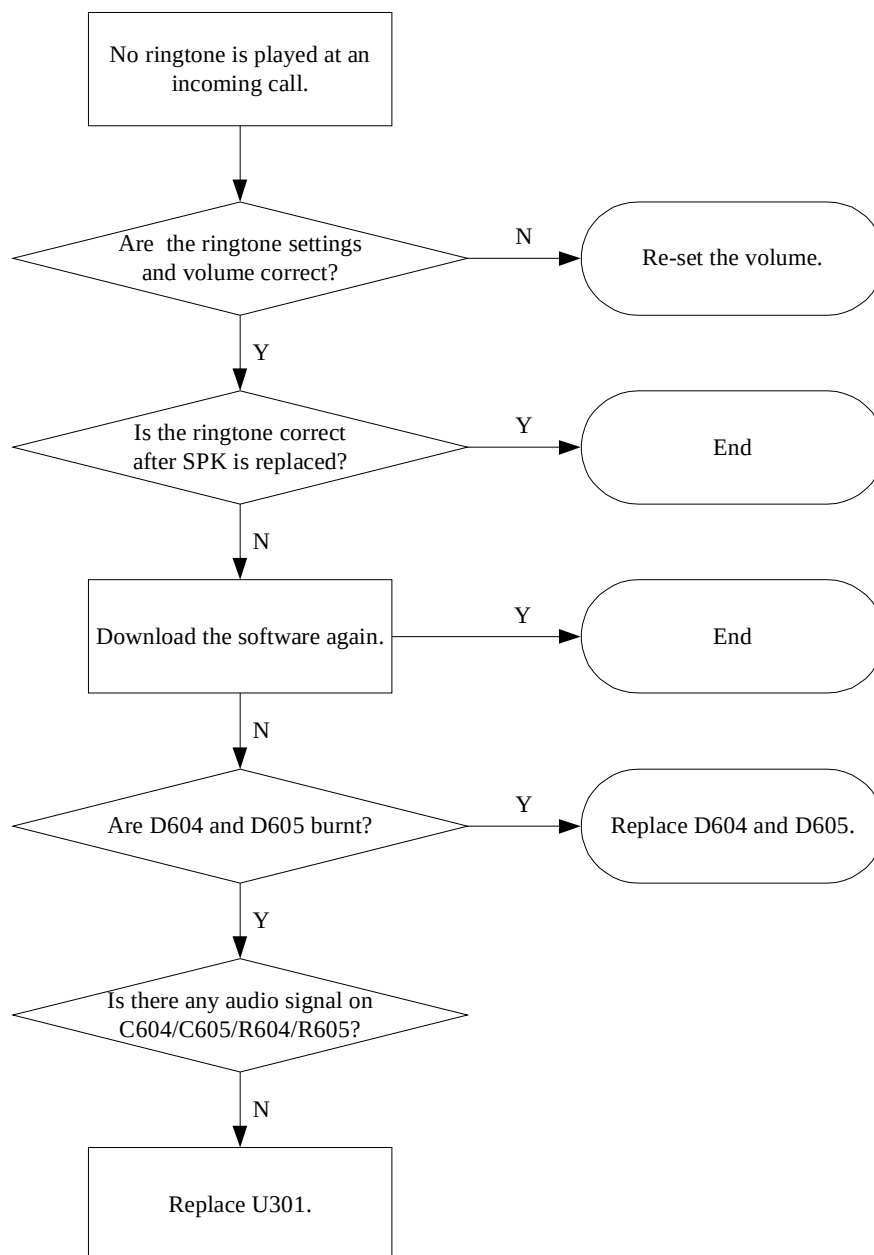
5.2 No Display of LCD



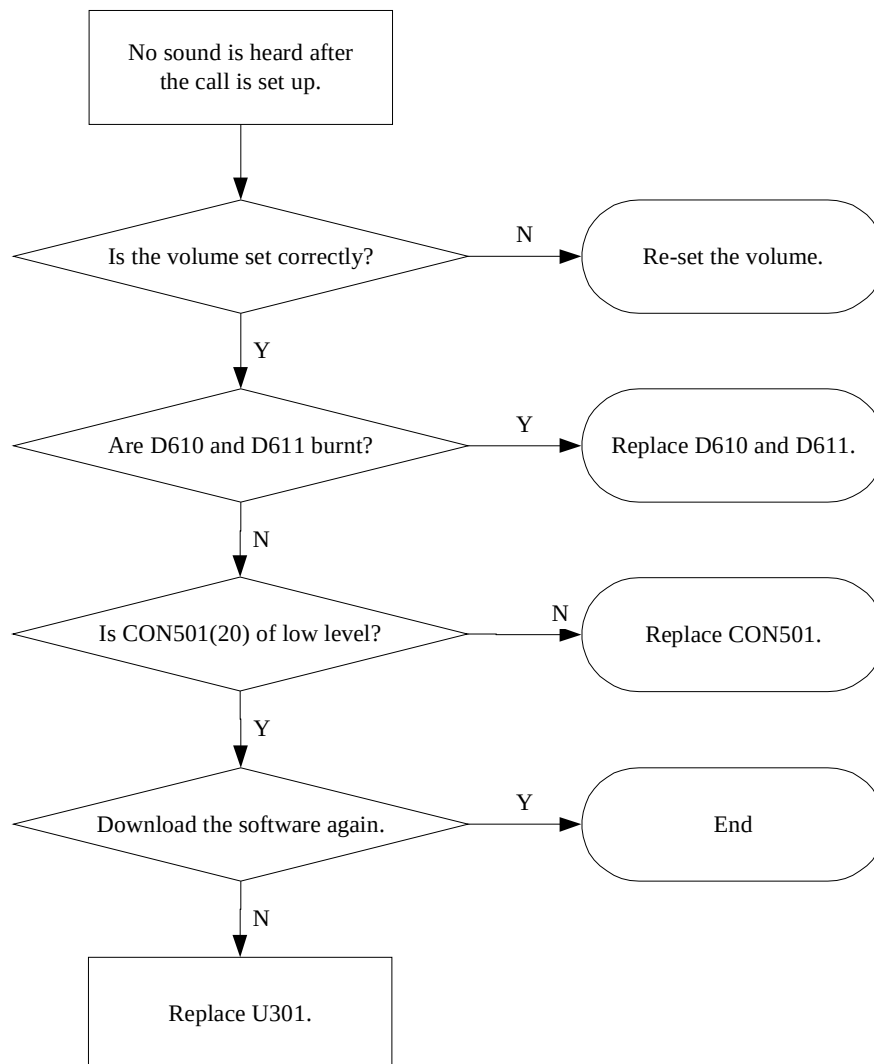
5.3 "Check UIM" is displayed after the phone is powered on.



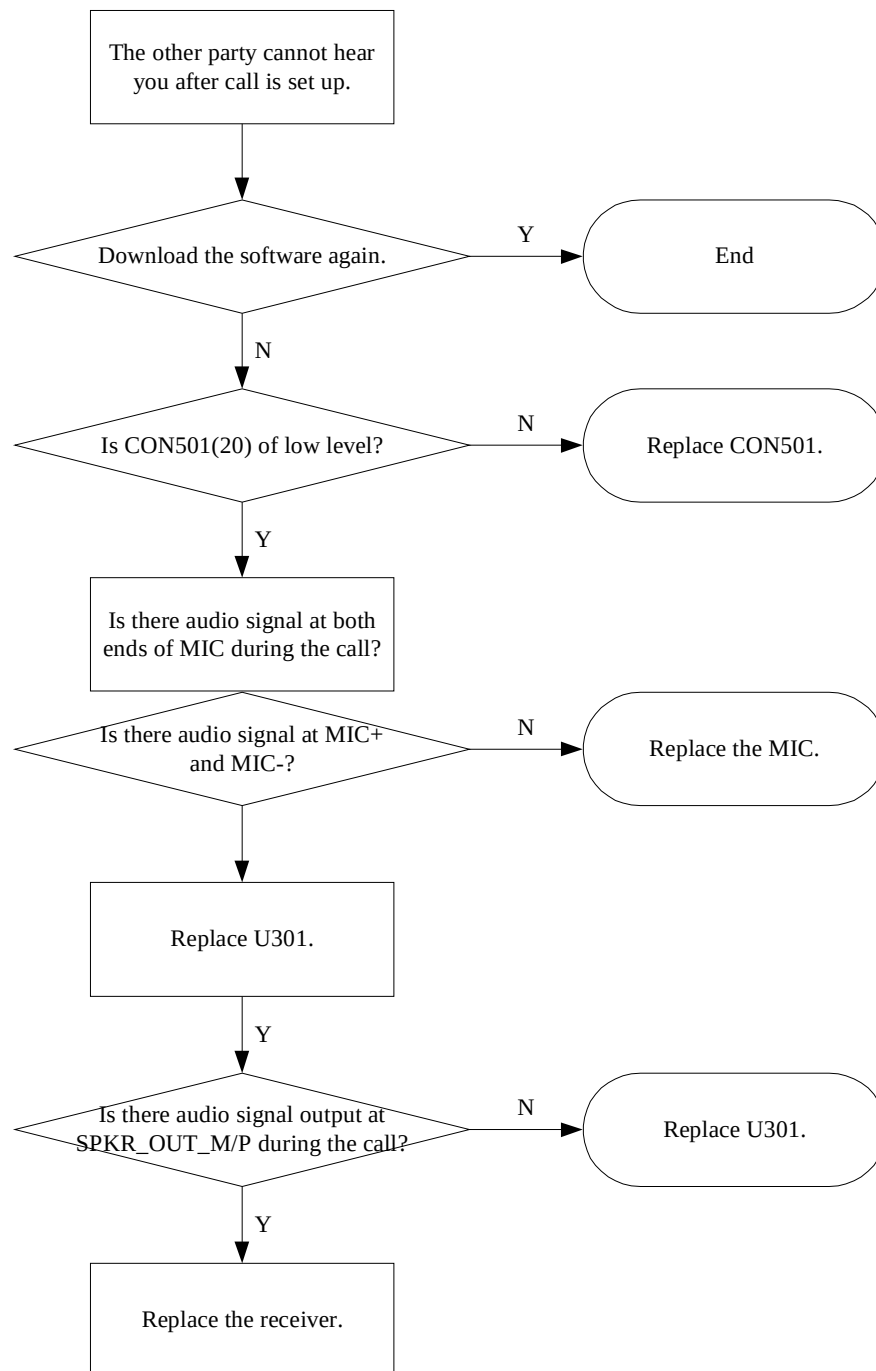
5.4 No Ringtone



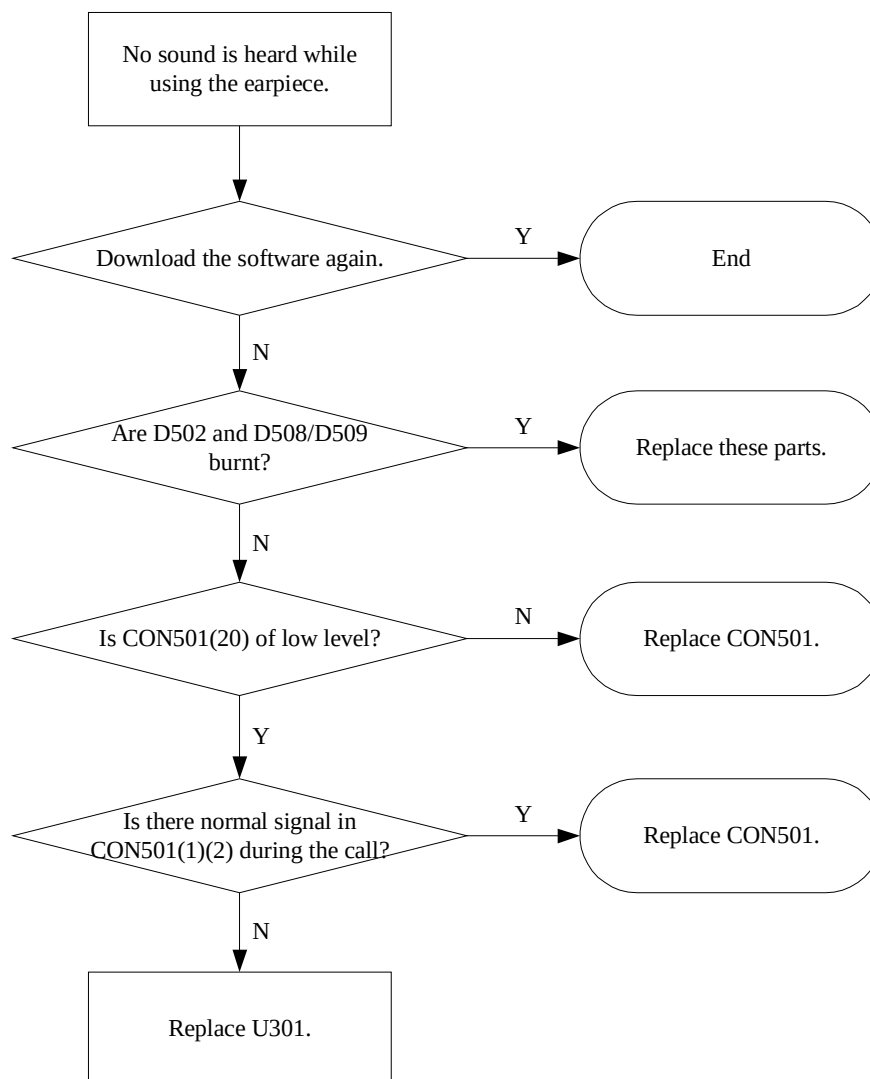
5.5 No sound is heard after the call is set up.



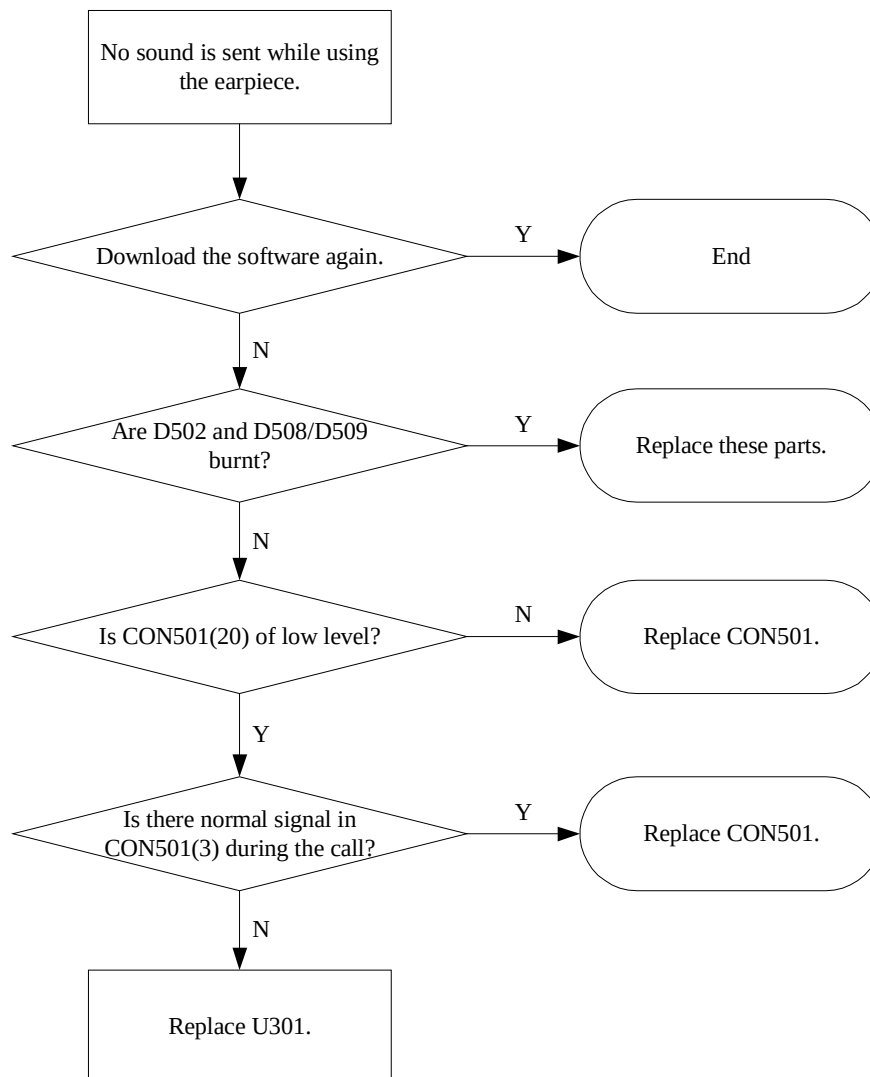
5.6 The other party cannot hear you after the call is set up.



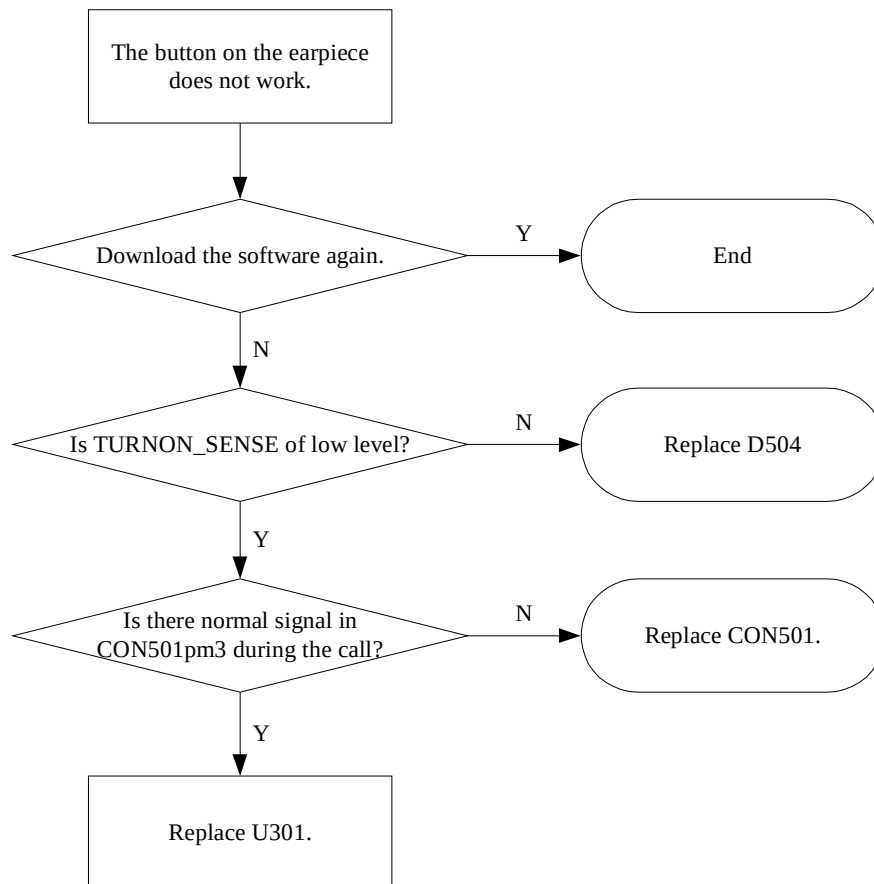
5.7 No sound is heard while using the earpiece.



5.8 No sound is sent while using the earpiece.



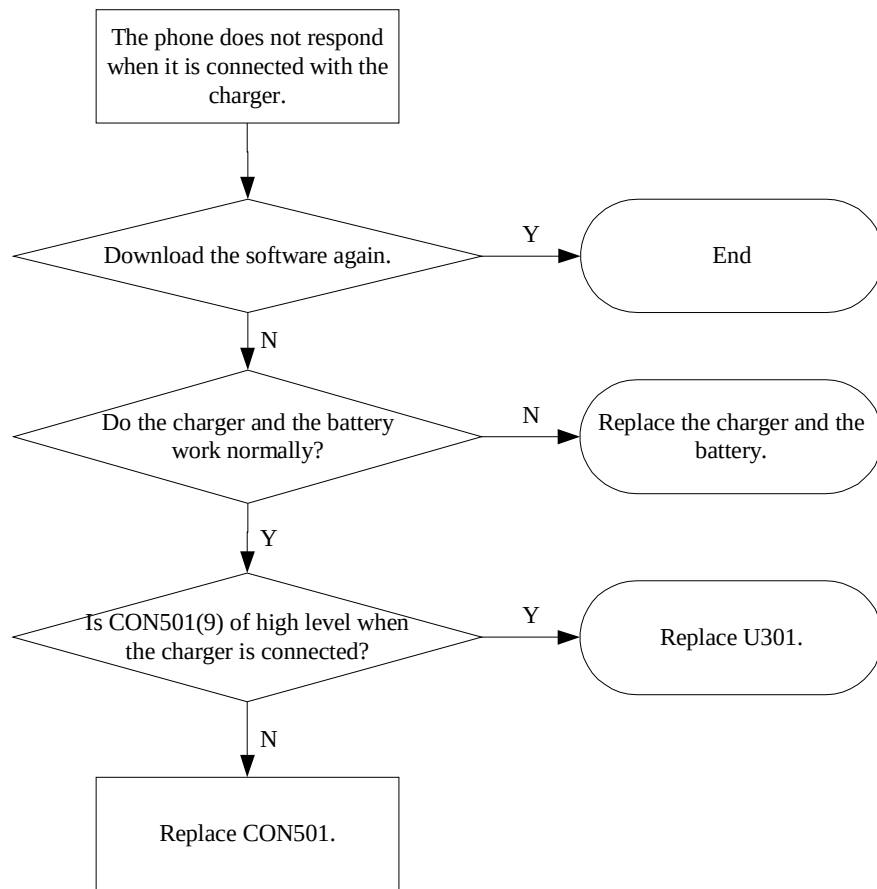
5.9 Press the button on the earpiece to answer a call is ineffective.



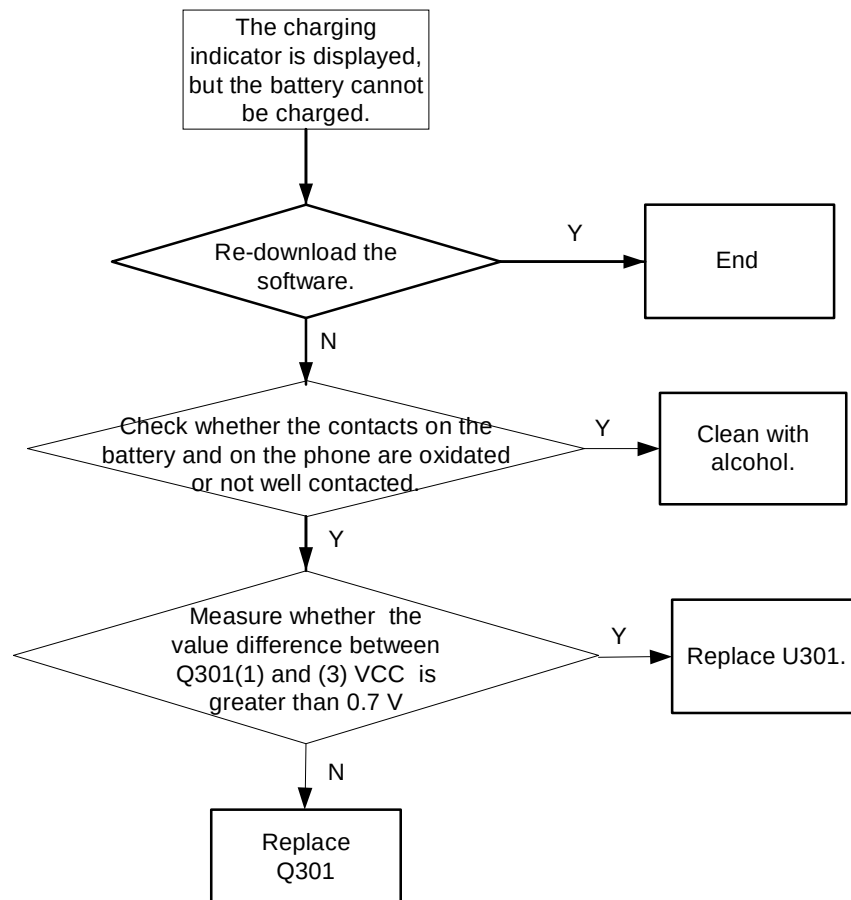
5.10 No Charging

The charging failures include the following two conditions: the phone does not respond when it is connected with the charger; or the charging indicator is displayed but the battery cannot be charged. To the phone cannot be charged, detect the I/O interface first to check whether there is obvious corruption.

The charging indicator is not displayed when the phone is connected with the charger.



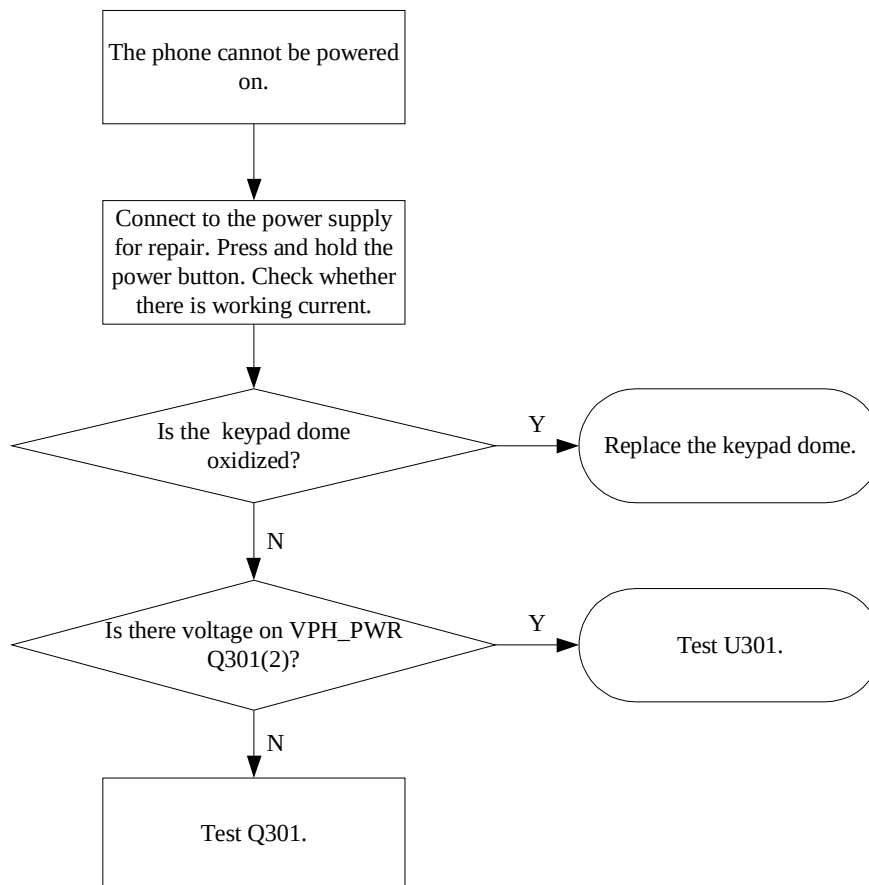
The charging indicator is displayed, but the battery cannot be charged.



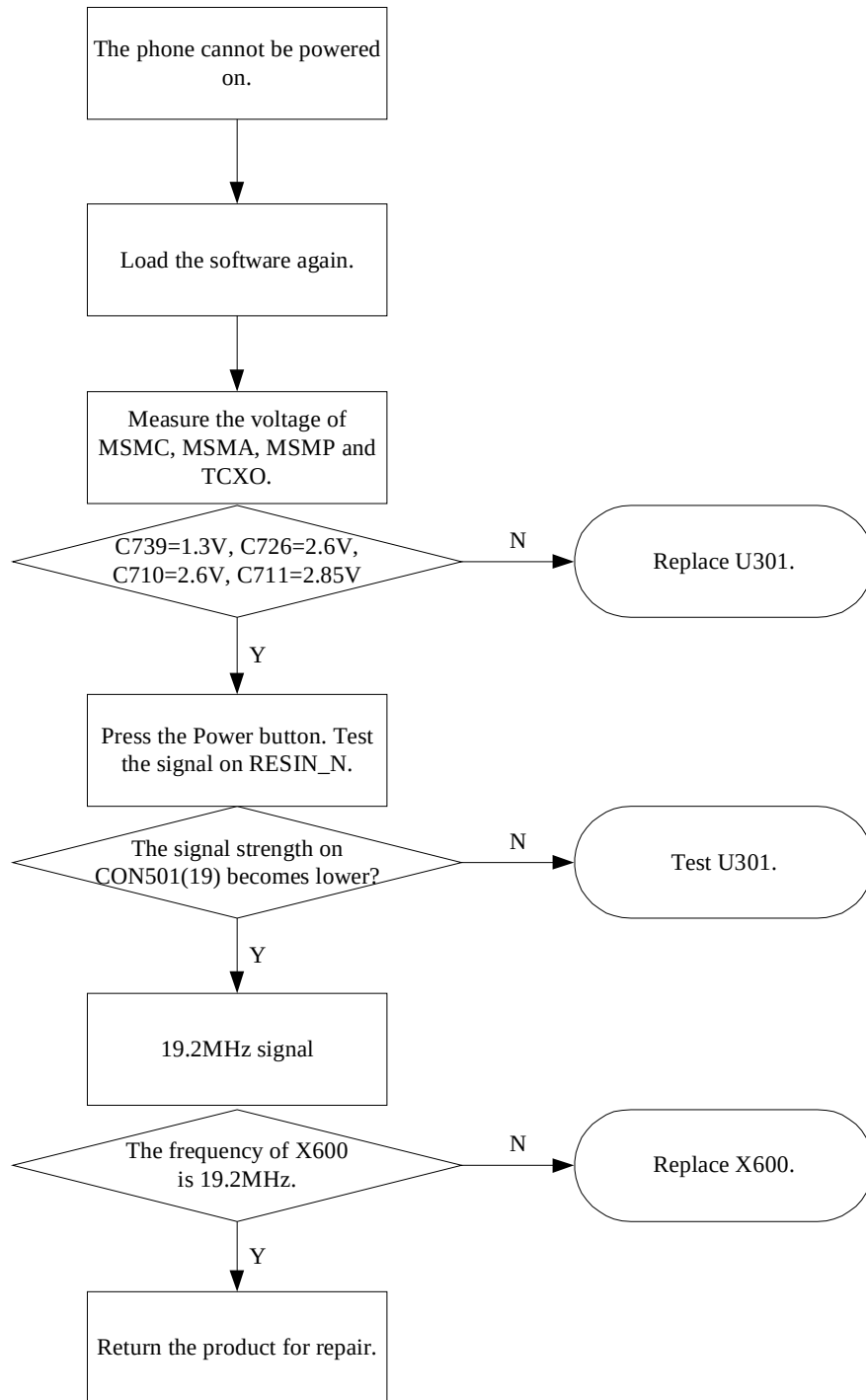
5.11 The phone cannot be powered on.

To the phone cannot be powered on, detect the I/O interface first to check whether there is obvious corruption. If the I/O interface is OK, power the phone with the stable DC power. Then detect the current of the phone according to the following conditions.

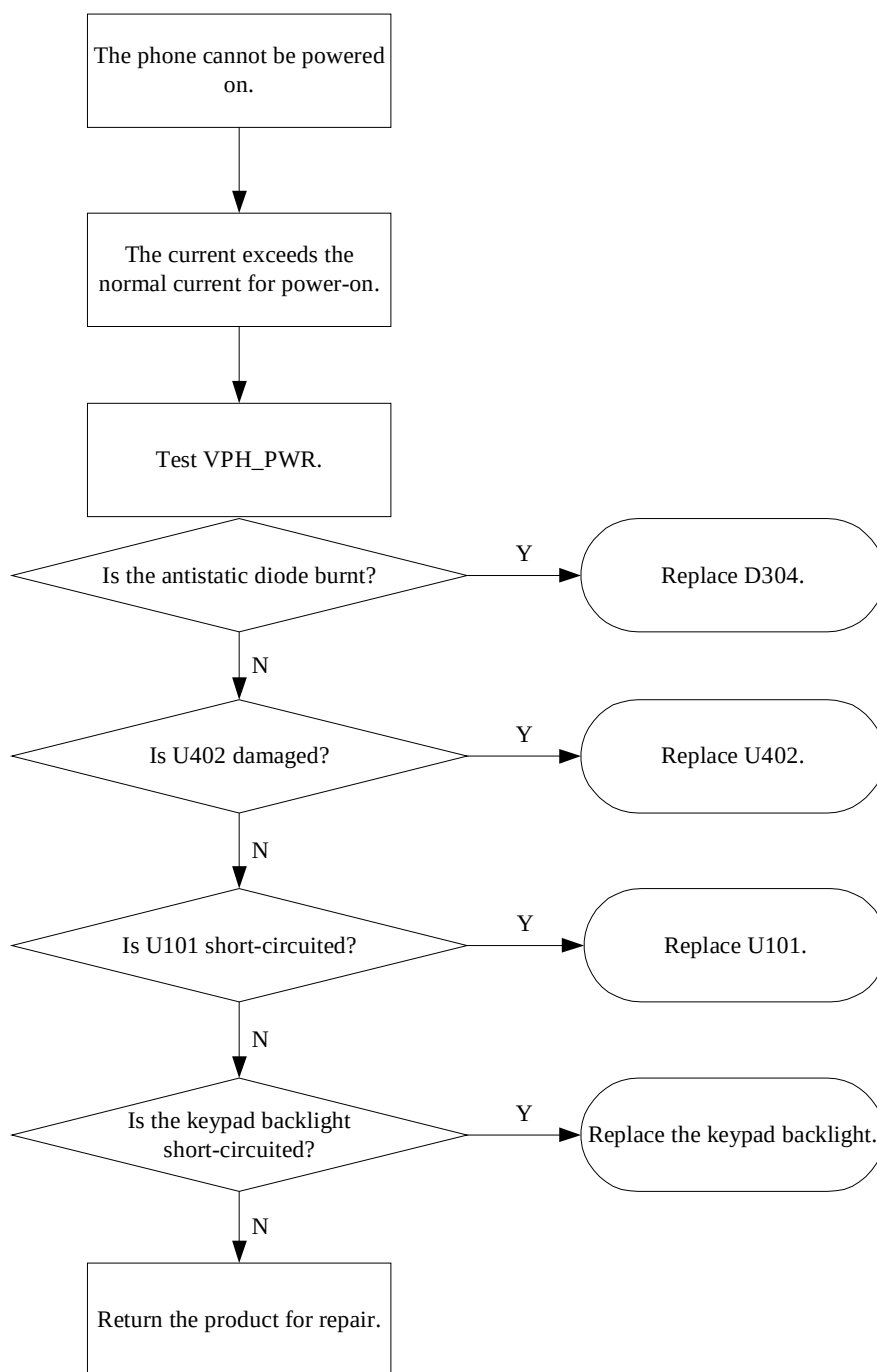
No Current



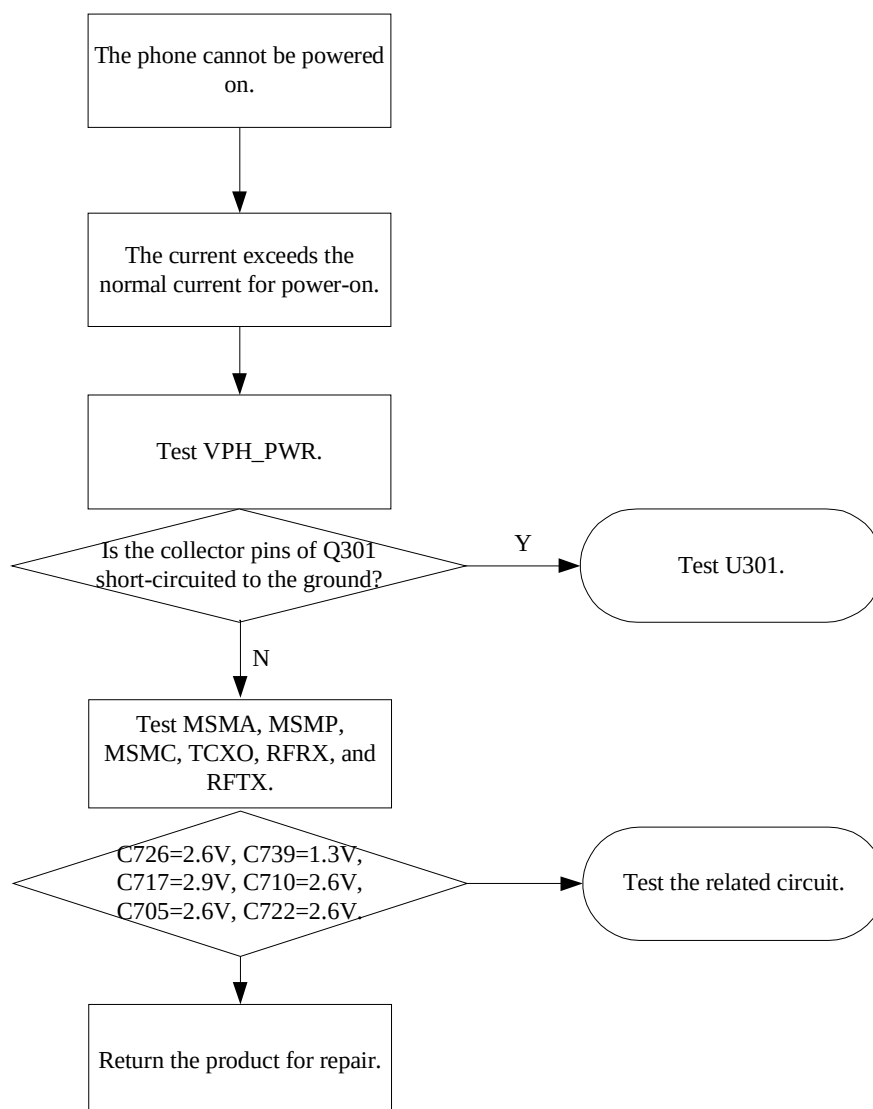
Small Current



Under stable voltage, the current of the phone becomes large without powering on.

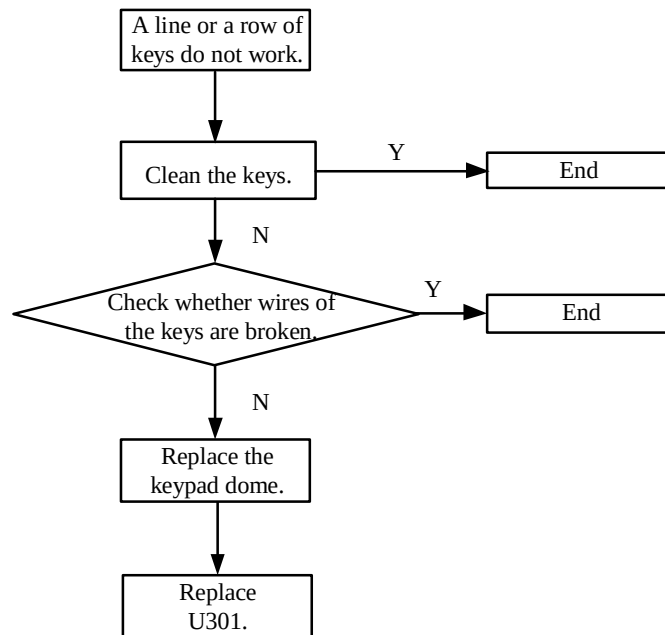


Under stable voltage, the current of the phone becomes large after it is powered on.

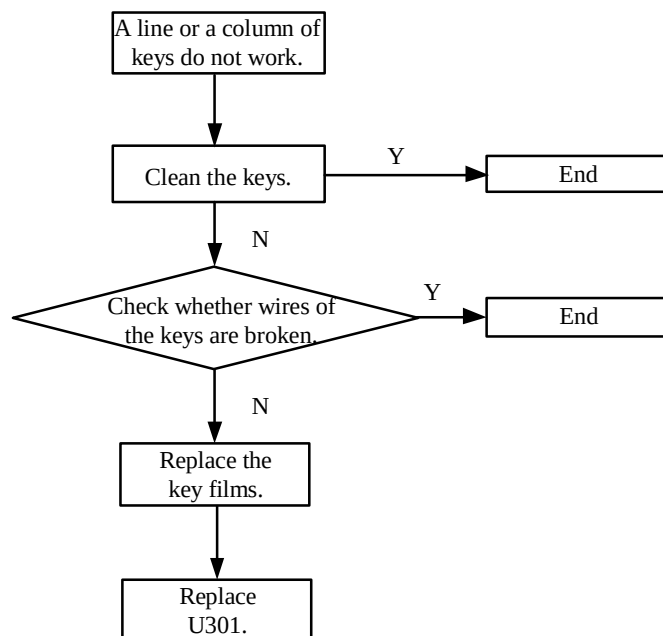


5.12 Key Failure

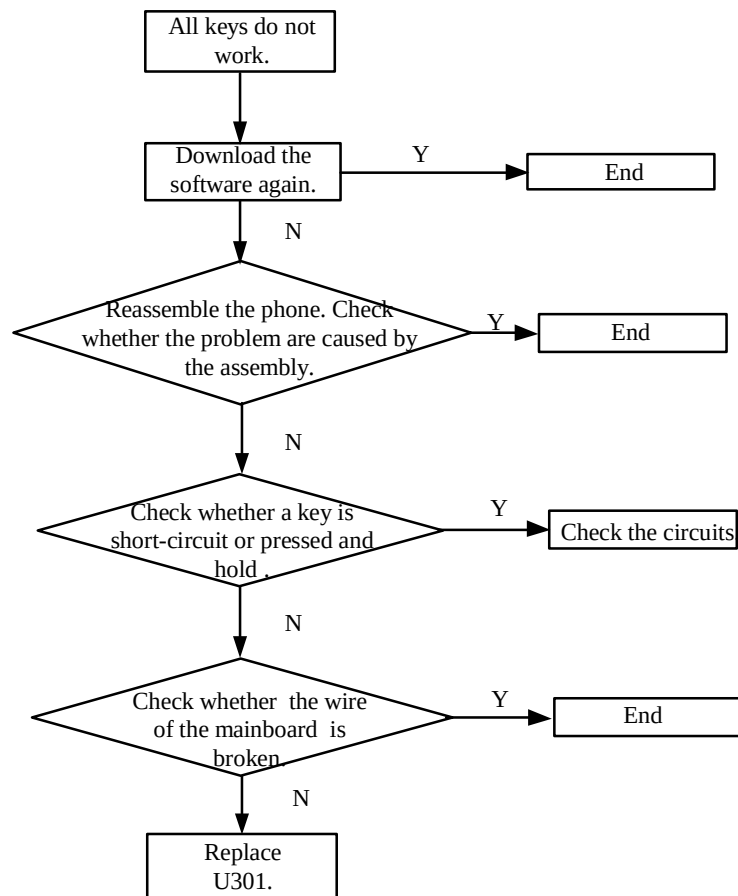
A single key does not work.



A line or a column of keys do not work.



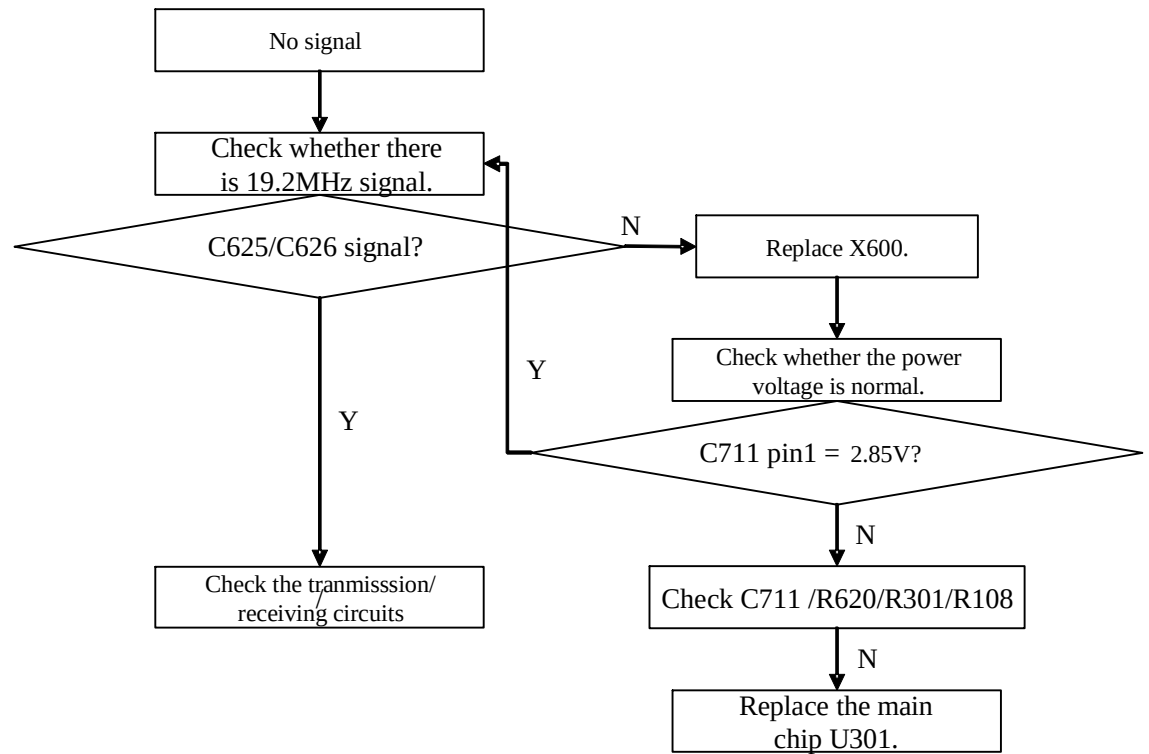
All keys do not work.



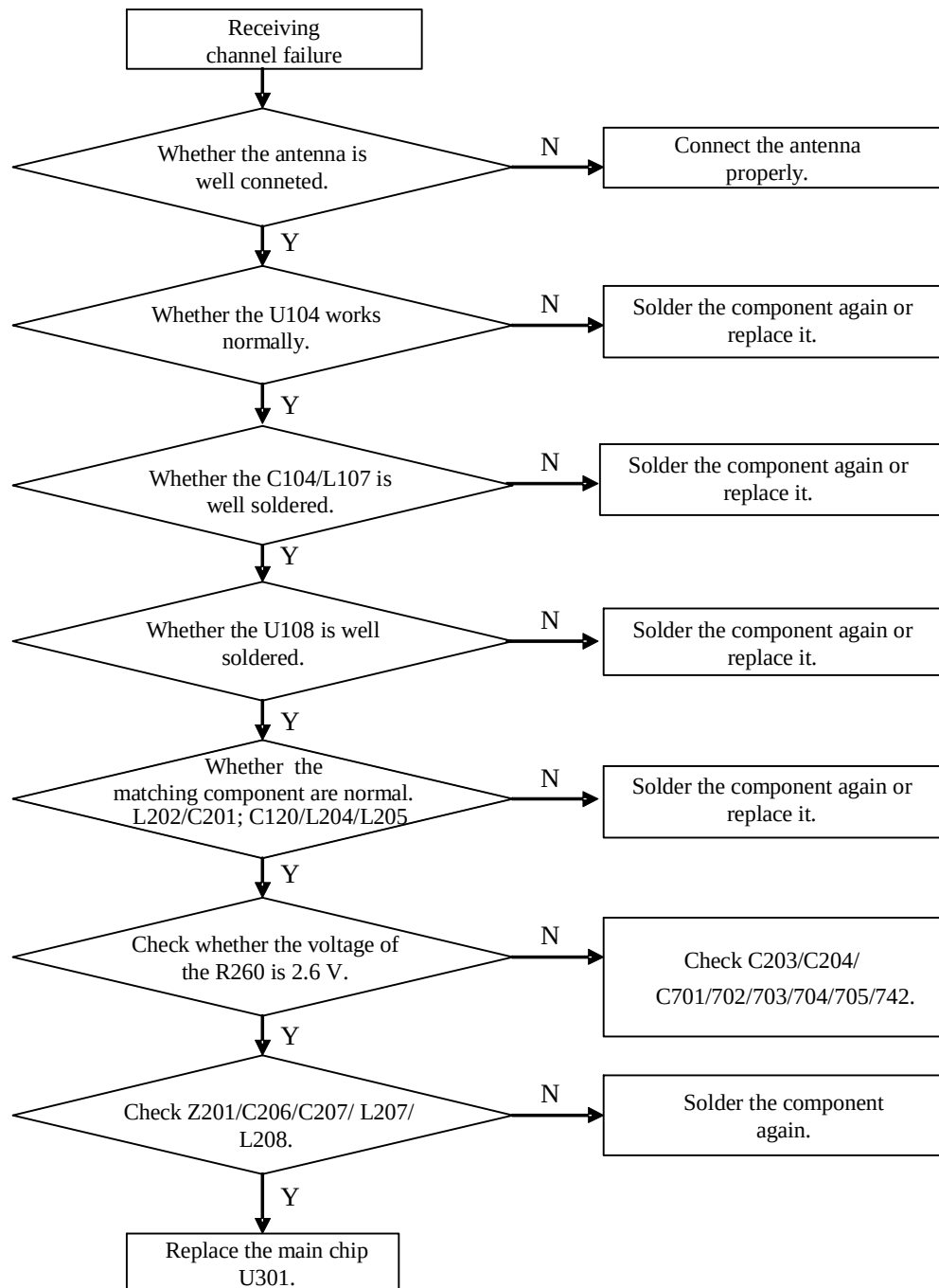
5.13 No Signal

Confirm the UIM card and the antenna are well contacted. Then detect according to the following flow.

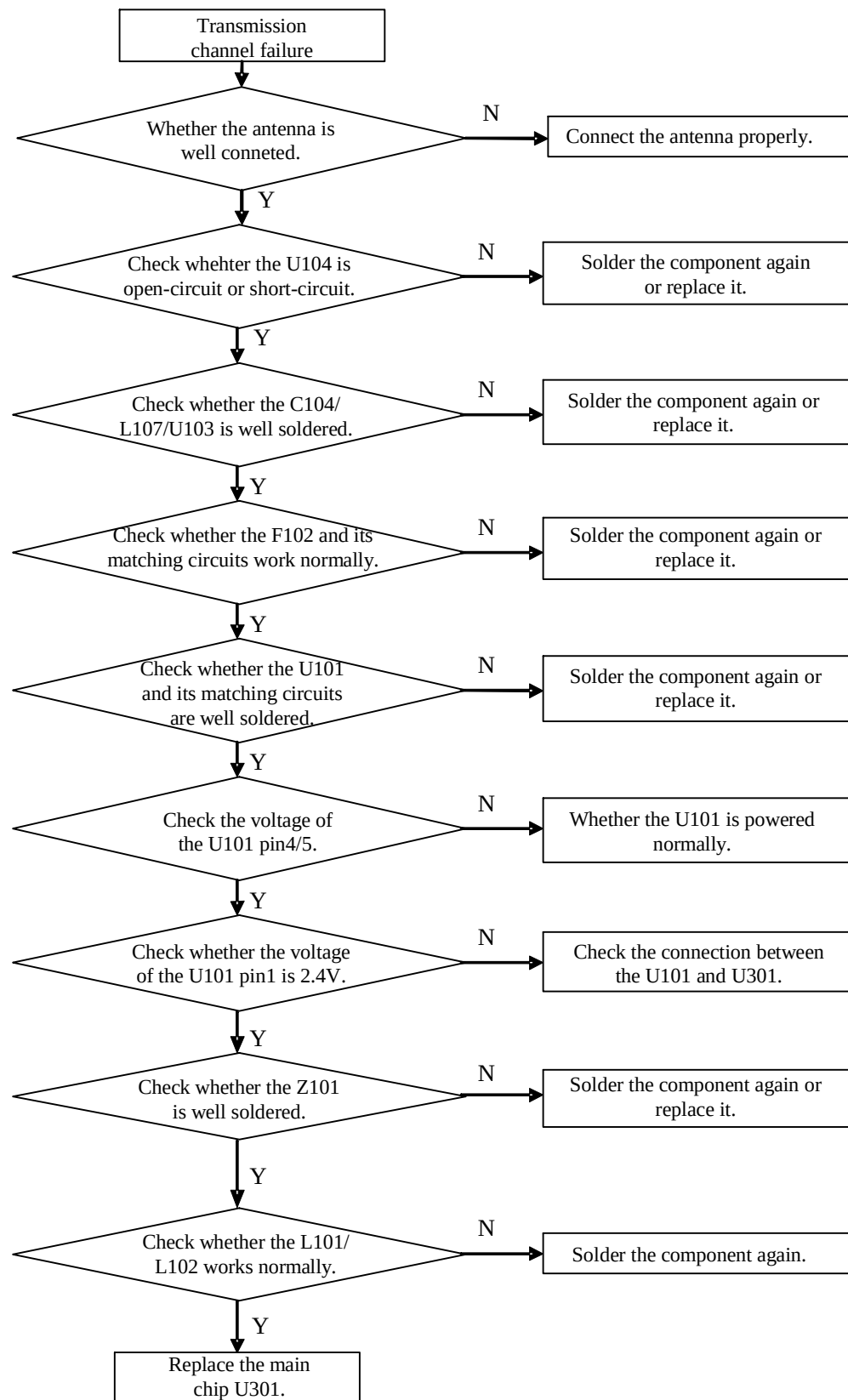
PLL Detection



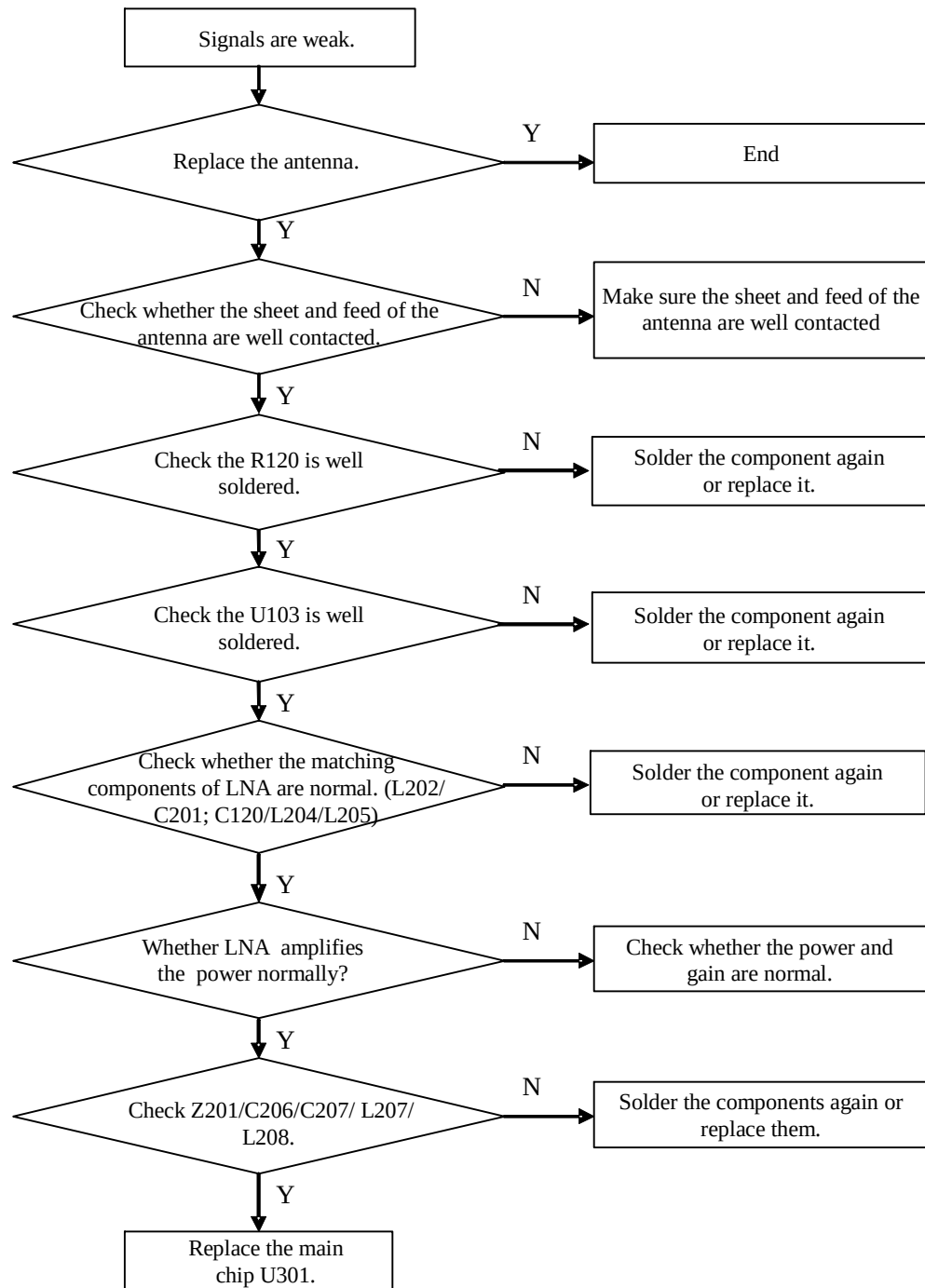
Receiving Channel



Transmission Channel

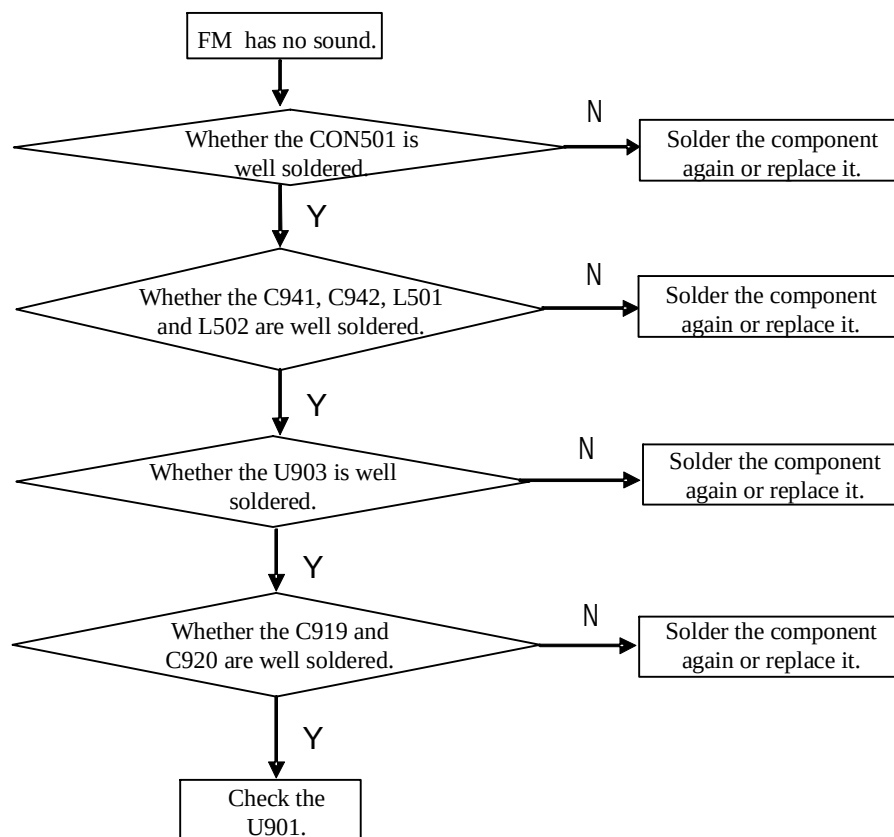


5.14 Weak Signal

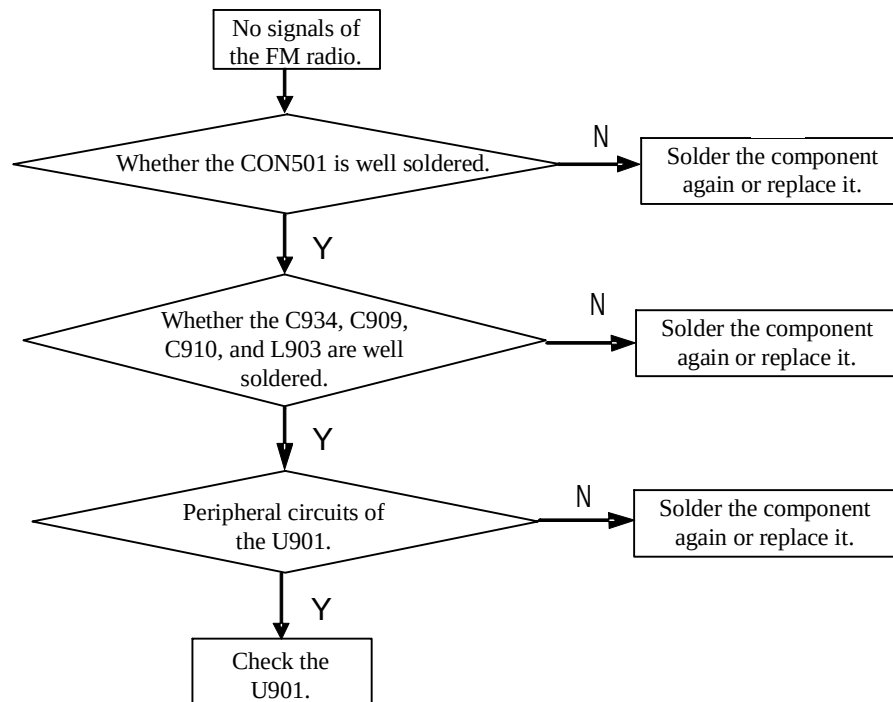


5.15 FM Failure

No sound



No Signal



6 Appendix

6.1 Unused Pad of the BGA

U301: QSC6010

A1,A2,A3,A19,A21,A22,	B1,B2,B3,B12,B18,B19,B22,	C1,C2,C22	D1,D2,D10,	E2,E8,E10,
F1 ,K13,L13	M2,M4,M5,M7,M8,M13	N2,N7,N12,N10	P5,	R4,R9,R13,R14
T1,T4,T7,T8,	V5,V7,V6,V8,	W7,W13,W18	U5 ,Y2,	AA1,AA22,AB1,AB2,AB7,AB16,AB17,AB21,AB22

U402: MEMORY IC

A1,A2,A7,A8,	B6,C3,C7,C5,	D3,E3,
J1, H8	G7,G8,K3, K6,K4, ,K2,	M1,M2,M7,M8

6.2 Networks to the Test Point

TS501	VEXT_DC (charger access)
TS502	UART1_TX_D (serial port transmission)
TS503	UART1_RX_D (serial port reception)
TS504	KPD_PWR_ON(power-on signal
TS505	GND (ground)

TS501	VEXT_DC (charger access)
TS506	V_BATT(battery voltage)
TS508	BATT_THERM (battery temperature detection)

6.3 Acronyms and Abbreviations

C	
CDMA	Code-Division Multiple Access
F	
FPC	Flexible Printed Circuit
FSTN	Fast super-twisted nematic
G	
GPIO	General-purpose Input/Output
L	
LCD	liquid crystal display
LCM	liquid crystal display module
LDO	Low-Drop Output regulator
LED	Light Emitting Diode
LNA	Low Noise Amplifier
P	
PM	Power Management
R	
Rx	Receive
R-UIM	Removable-User Identity Module
S	
SBI	Serial Bus Interface
SMPL	Sudden Momentary Power Loss
T	
Tx	Transmit
U	
USB	universal serial bus

